FIG. 1

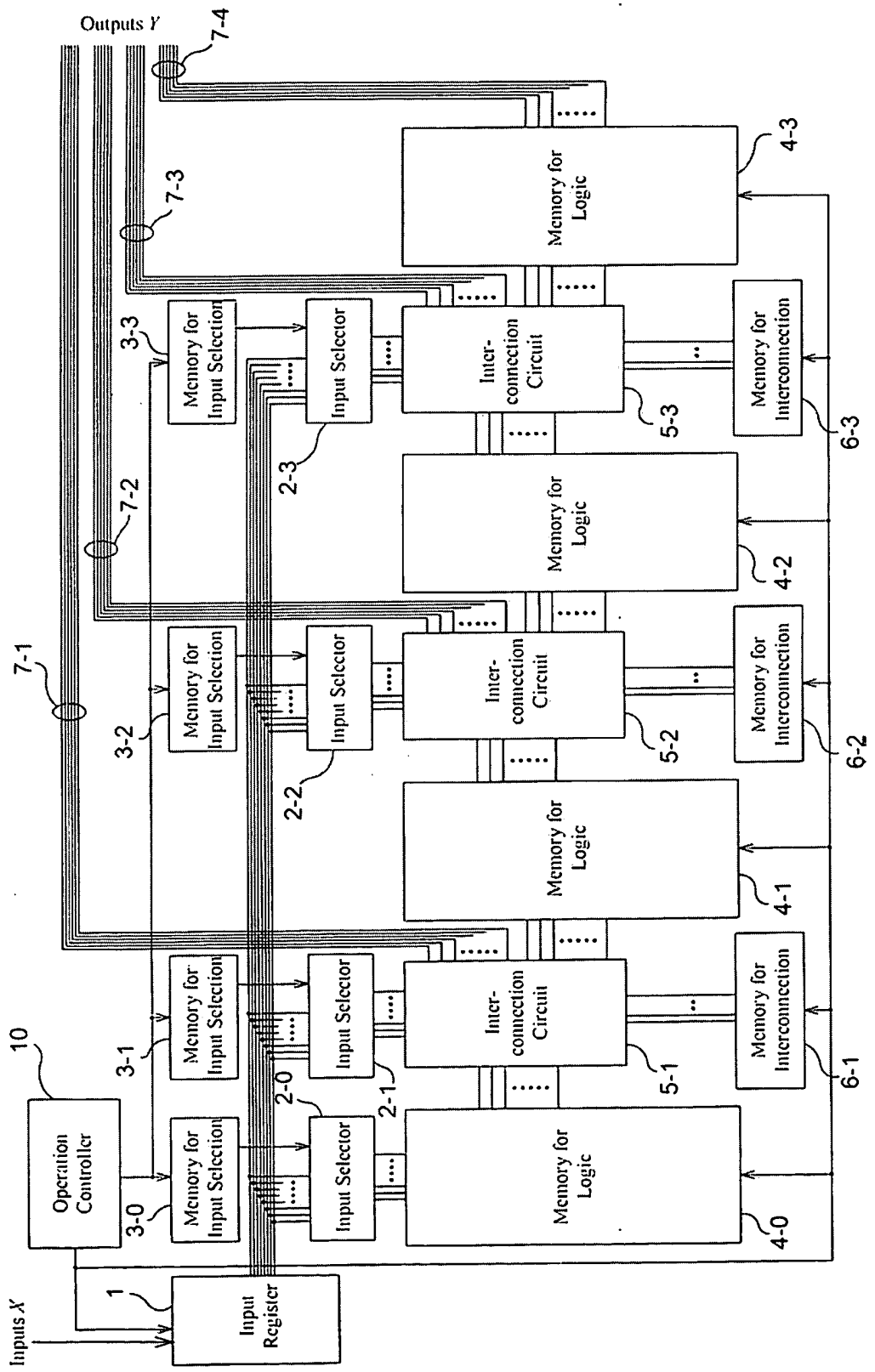

Outputs Y
7-4
7-3
7-2
7-1
Memory for Logic
4-3
Memory for Input Selection
3-3
Input Selector
2-3
Inter-connection Circuit
5-3
Memory for Interconnection
6-3
Memory for Logic
4-2
Memory for Input Selection
3-2
Input Selector
2-2
Inter-connection Circuit
5-2
Memory for Interconnection
6-2
Memory for Logic
4-1
Memory for Input Selection
3-1
Input Selector
2-1
Inter-connection Circuit
5-1
Memory for Interconnection
6-1
Operation Controller
10
Memory for Input Selection
3-0
Input Selector
2-0
Memory for Logic
4-0
Inputs X
1
Input Register

FIG. 2

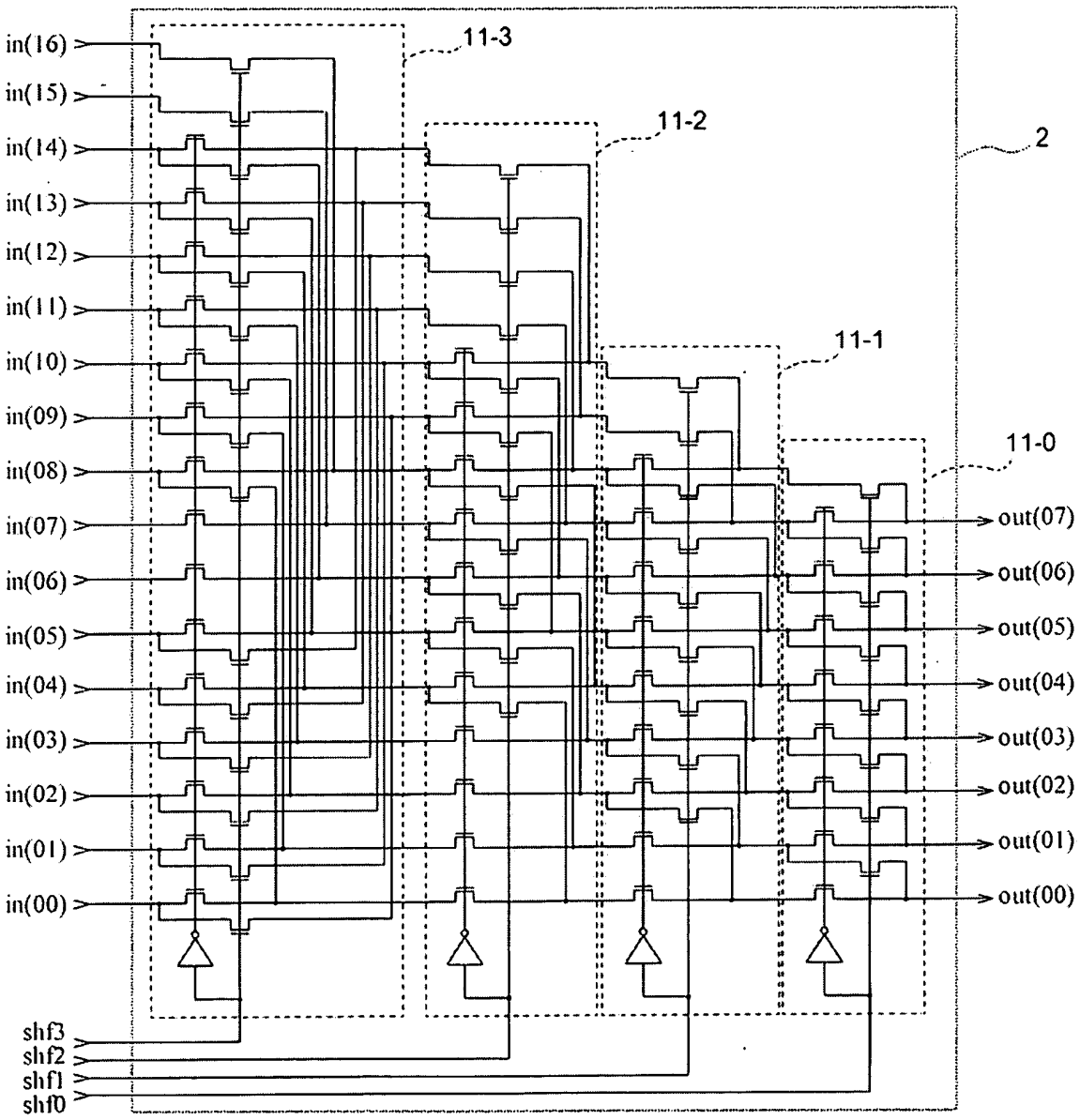

in(16)
in(15)
in(14)
in(13)
in(12)
in(11)
in(10)
in(09)
in(08)
in(07)
in(06)
in(05)
in(04)
in(03)
in(02)
in(01)
in(00)
shf3
shf2
shf1
shf0
11-3
11-2
11-1
11-0
2
out(07)
out(06)
out(05)
out(04)
out(03)
out(02)
out(01)
out(00)

FIG. 3

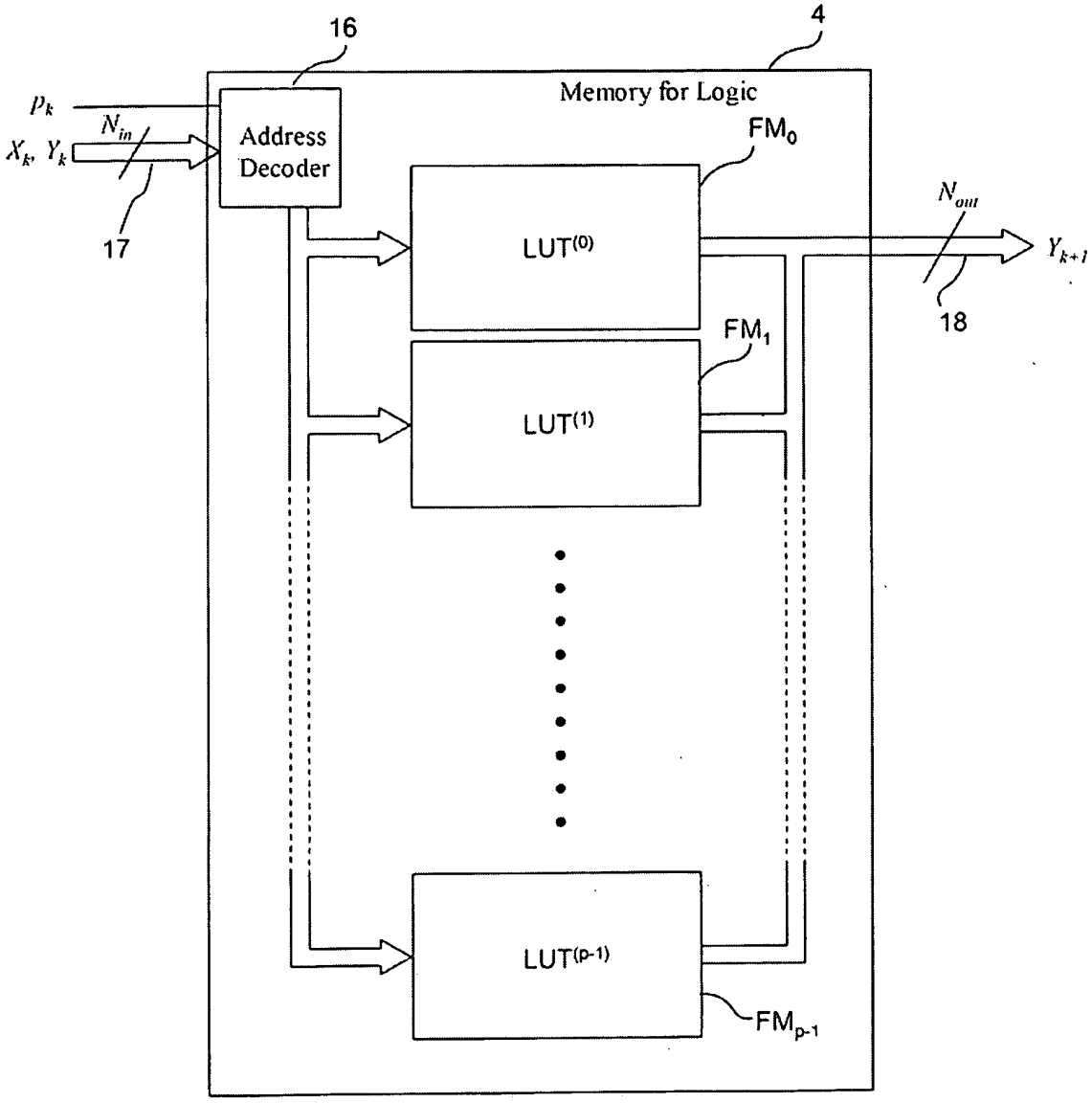

16
4
Memory for Logic
p_k
N_{in}
X_k, Y_k
Address Decoder
17
FM_0
$LUT^{(0)}$
N_{out}
Y_{k+1}
18
FM_1
$LUT^{(1)}$
$LUT^{(p-1)}$
FM_{p-1}

FIG. 4

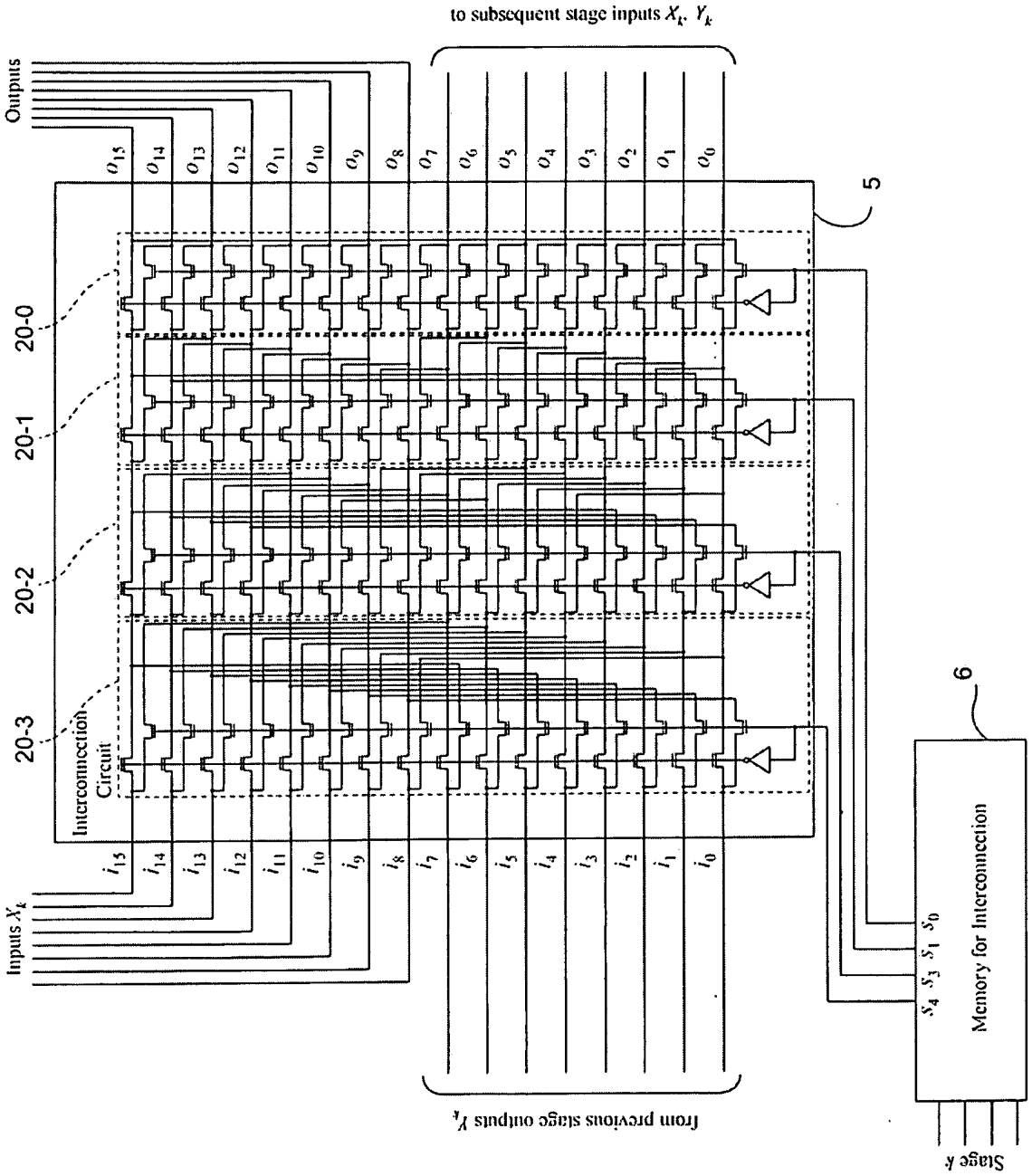

to subsequent stage inputs X_k, Y_k
Outputs
o_{15} o_{14} o_{13} o_{12} o_{11} o_{10} o_9 o_8 o_7 o_6 o_5 o_4 o_3 o_2 o_1 o_0
5
20-0
20-1
20-2
20-3
Interconnection Circuit
i_{15} i_{14} i_{13} i_{12} i_{11} i_{10} i_9 i_8 i_7 i_6 i_5 i_4 i_3 i_2 i_1 i_0
Inputs X_k
from previous stage outputs Y_k
6
s_4 s_3 s_1 s_0
Memory for Interconnection
Stage k

FIG. 5

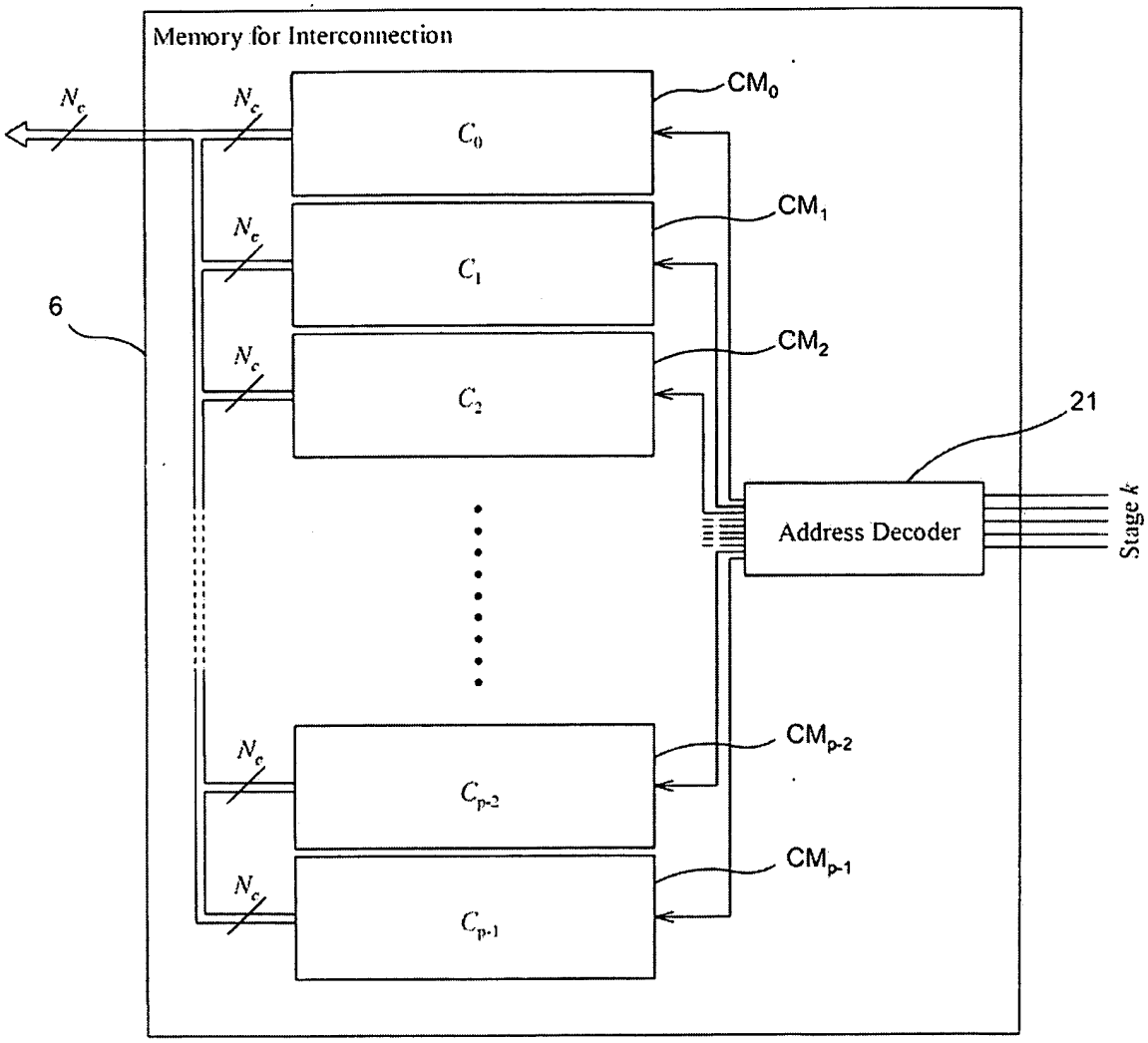

Memory for Interconnection
N_c
N_c
C_0
CM_0
N_c
C_1
CM_1
6
N_c
C_2
CM_2
21
Address Decoder
Stage k
N_c
C_{p-2}
CM_{p-2}
N_c
C_{p-1}
CM_{p-1}

FIG. 6

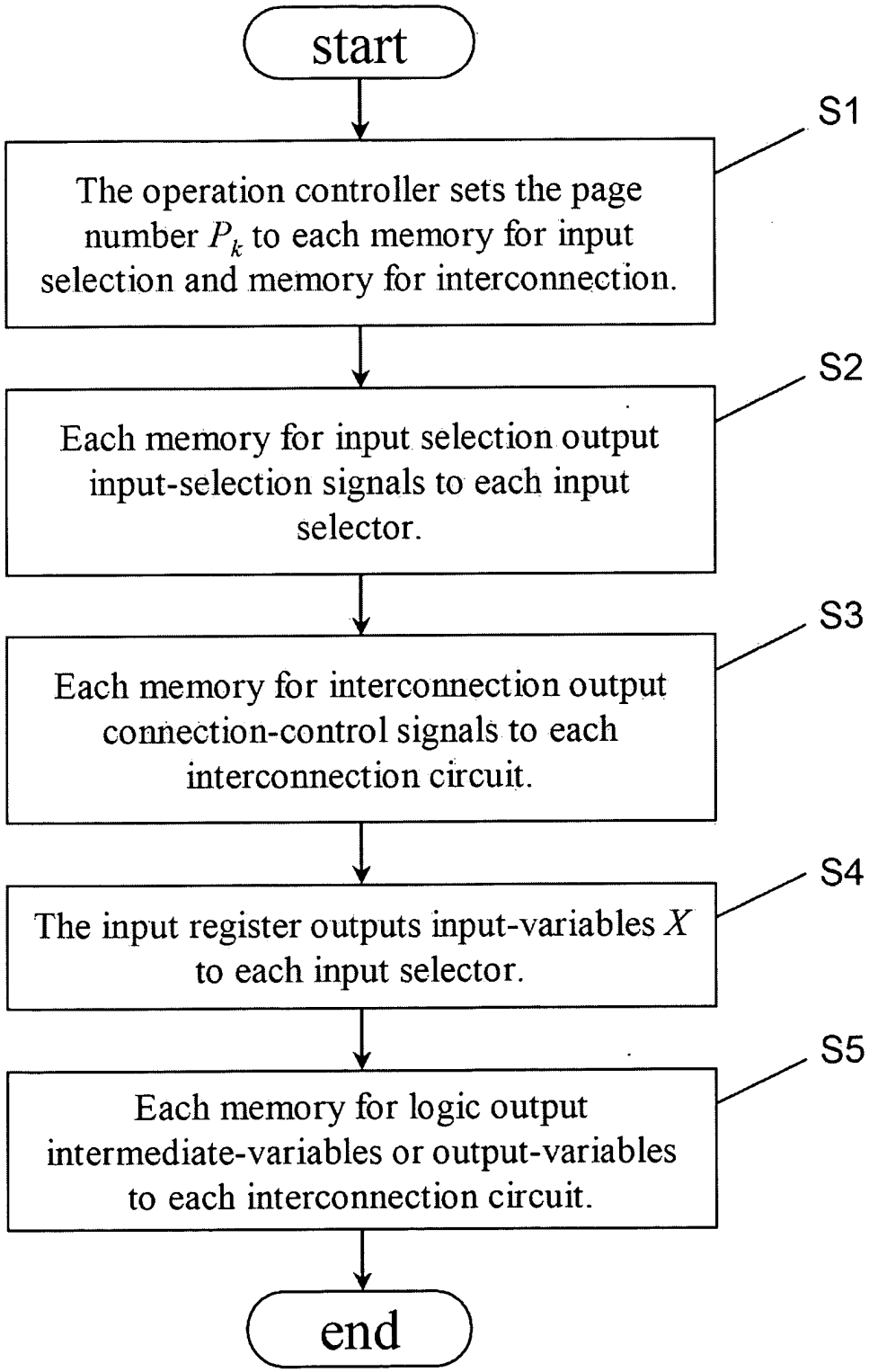

start
S1
The operation controller sets the page number P_k to each memory for input selection and memory for interconnection.
S2
Each memory for input selection output input-selection signals to each input selector.
S3
Each memory for interconnection output connection-control signals to each interconnection circuit.
S4
The input register outputs input-variables X to each input selector.
S5
Each memory for logic output intermediate-variables or output-variables to each interconnection circuit.
end

FIG. 7

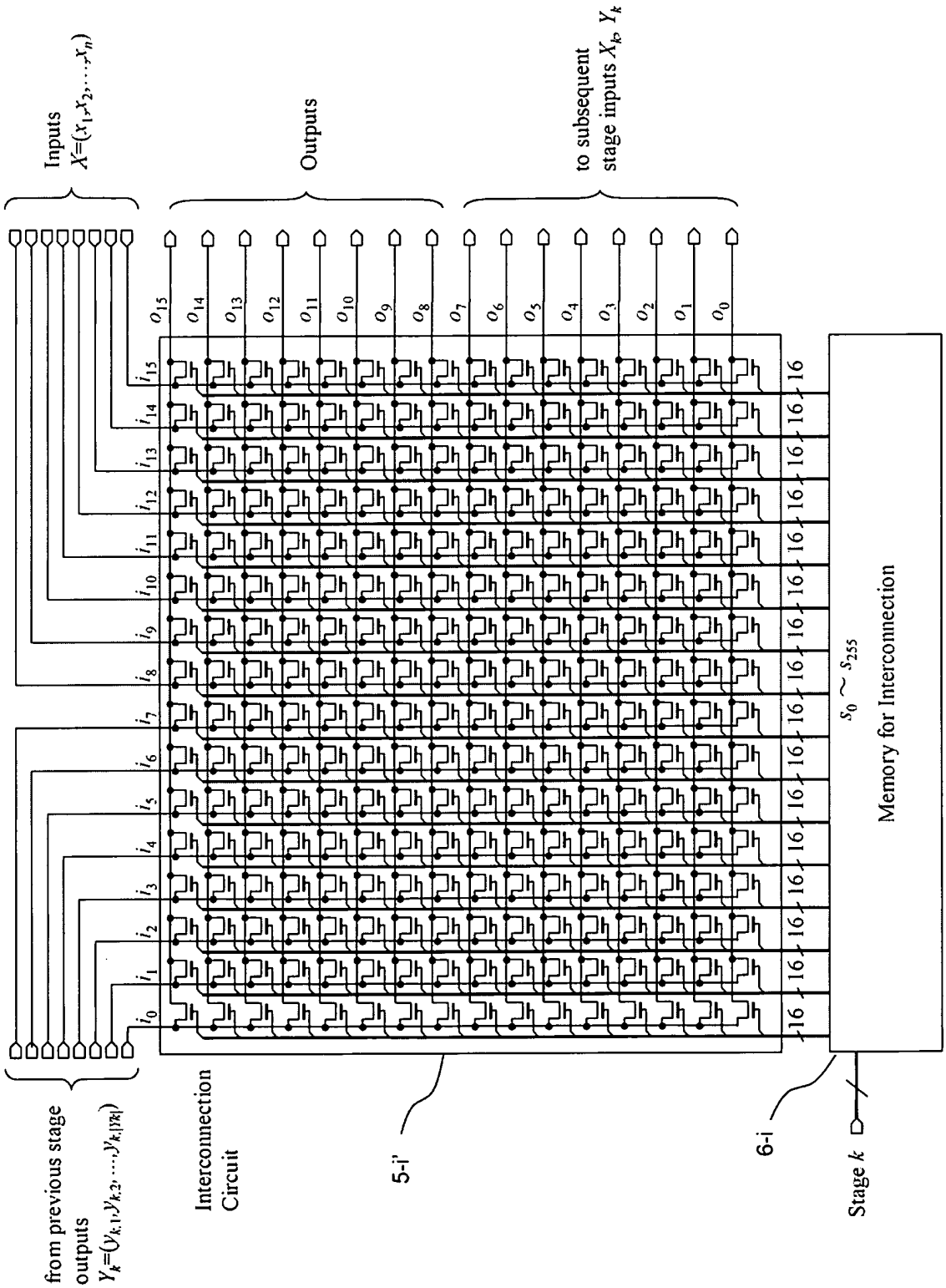

Inputs
$X=(x_1,x_2,\ldots,x_n)$
Outputs
to subsequent
stage inputs X_k, Y_k
o_{15} o_{14} o_{13} o_{12} o_{11} o_{10} o_9 o_8 o_7 o_6 o_5 o_4 o_3 o_2 o_1 o_0
i_{15} i_{14} i_{13} i_{12} i_{11} i_{10} i_9 i_8 i_7 i_6 i_5 i_4 i_3 i_2 i_1 i_0
16
$s_0 \sim s_{255}$
Memory for Interconnection
from previous stage
outputs
$Y_k=(y_{k,1},y_{k,2},\ldots,y_{k,|Yk|})$
Interconnection
Circuit
5-i'
6-i
Stage k

FIG. 8

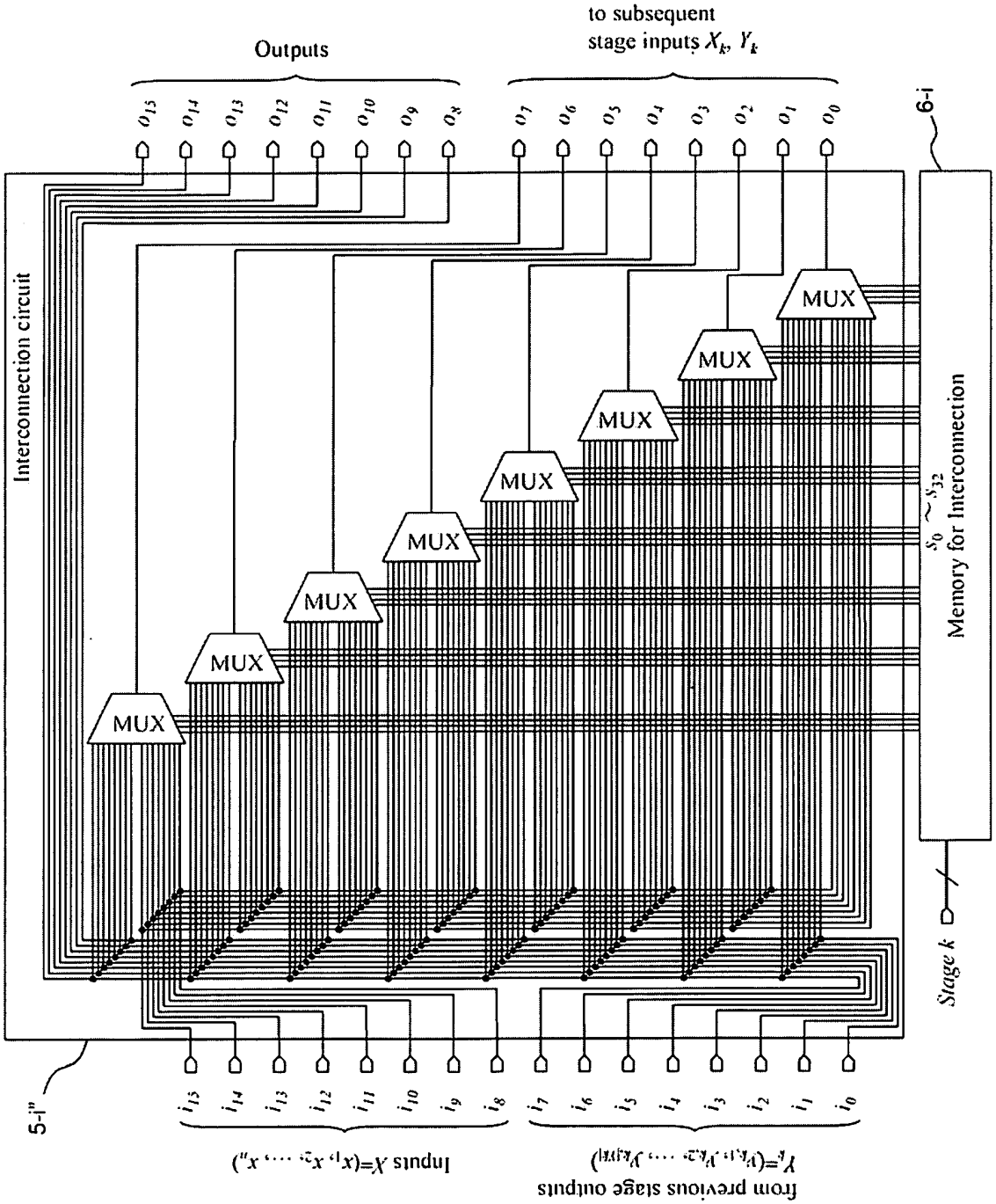

Outputs
to subsequent
stage inputs X_k, Y_k
o_{15} o_{14} o_{13} o_{12} o_{11} o_{10} o_9 o_8
o_7 o_6 o_5 o_4 o_3 o_2 o_1 o_0
6-i
Interconnection circuit
MUX
MUX
MUX
MUX
MUX
MUX
MUX
$s_0 \sim s_{32}$
Memory for Interconnection
Stage k
5-i"
i_{15} i_{14} i_{13} i_{12} i_{11} i_{10} i_9 i_8
i_7 i_6 i_5 i_4 i_3 i_2 i_1 i_0
Inputs $X=(x_1, x_2, \ldots, x_n)$
from previous stage outputs
$Y_k=(y_{k,1}, y_{k,2}, \ldots, y_{k,m})$

FIG. 9

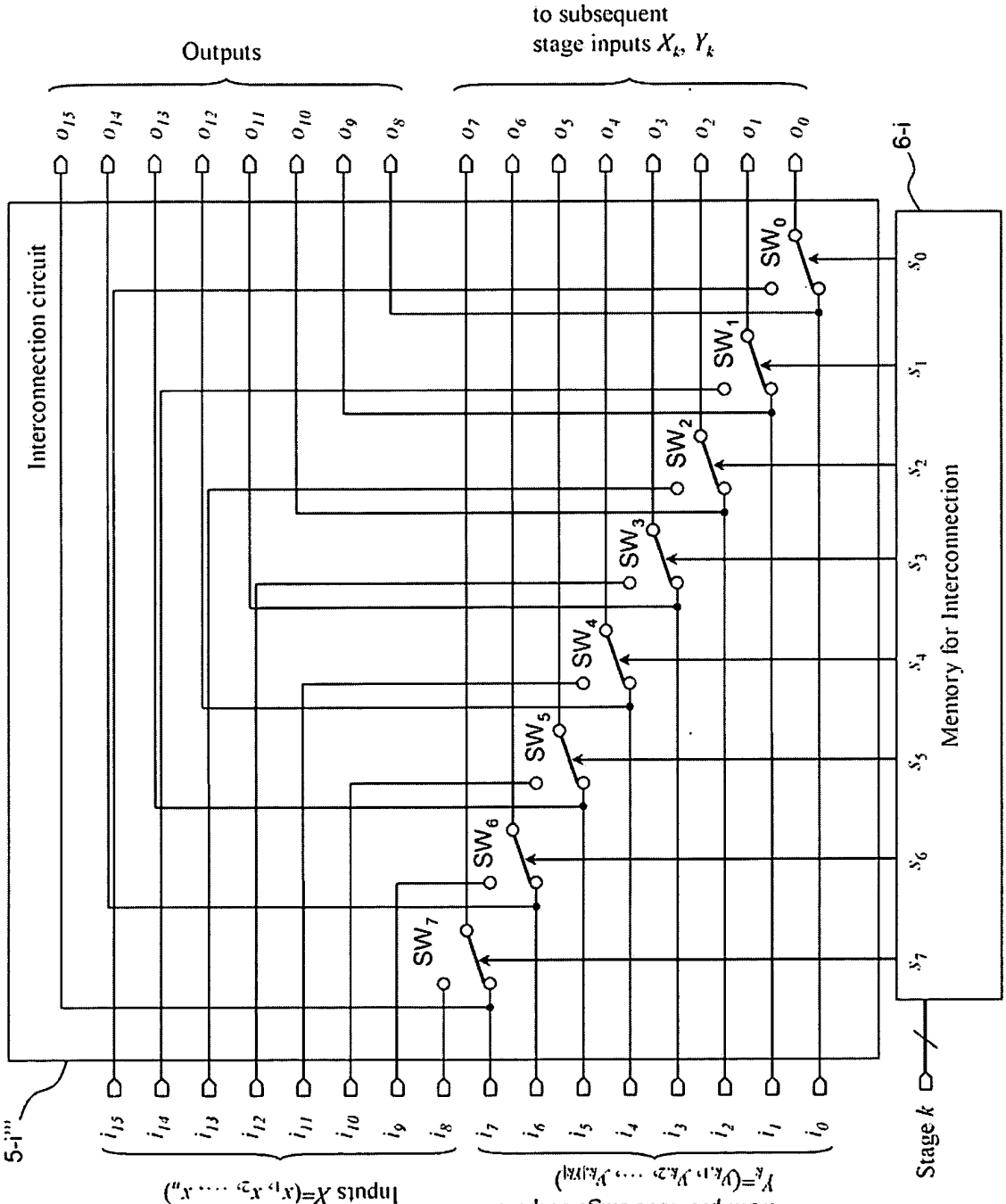

to subsequent
stage inputs X_k, Y_k
Outputs
o_{15} o_{14} o_{13} o_{12} o_{11} o_{10} o_9 o_8 o_7 o_6 o_5 o_4 o_3 o_2 o_1 o_0
6-i
Interconnection circuit
SW_0 SW_1 SW_2 SW_3 SW_4 SW_5 SW_6 SW_7
s_0 s_1 s_2 s_3 s_4 s_5 s_6 s_7
Memory for Interconnection
5-i
i_{15} i_{14} i_{13} i_{12} i_{11} i_{10} i_9 i_8 i_7 i_6 i_5 i_4 i_3 i_2 i_1 i_0
Stage k
Inputs $X=(x_1, x_2, \cdots, x_n)$
from previous stage outputs
$Y_k=(y_{k,1}, y_{k,2}, \cdots, y_{k,|Y_k|})$

FIG. 10

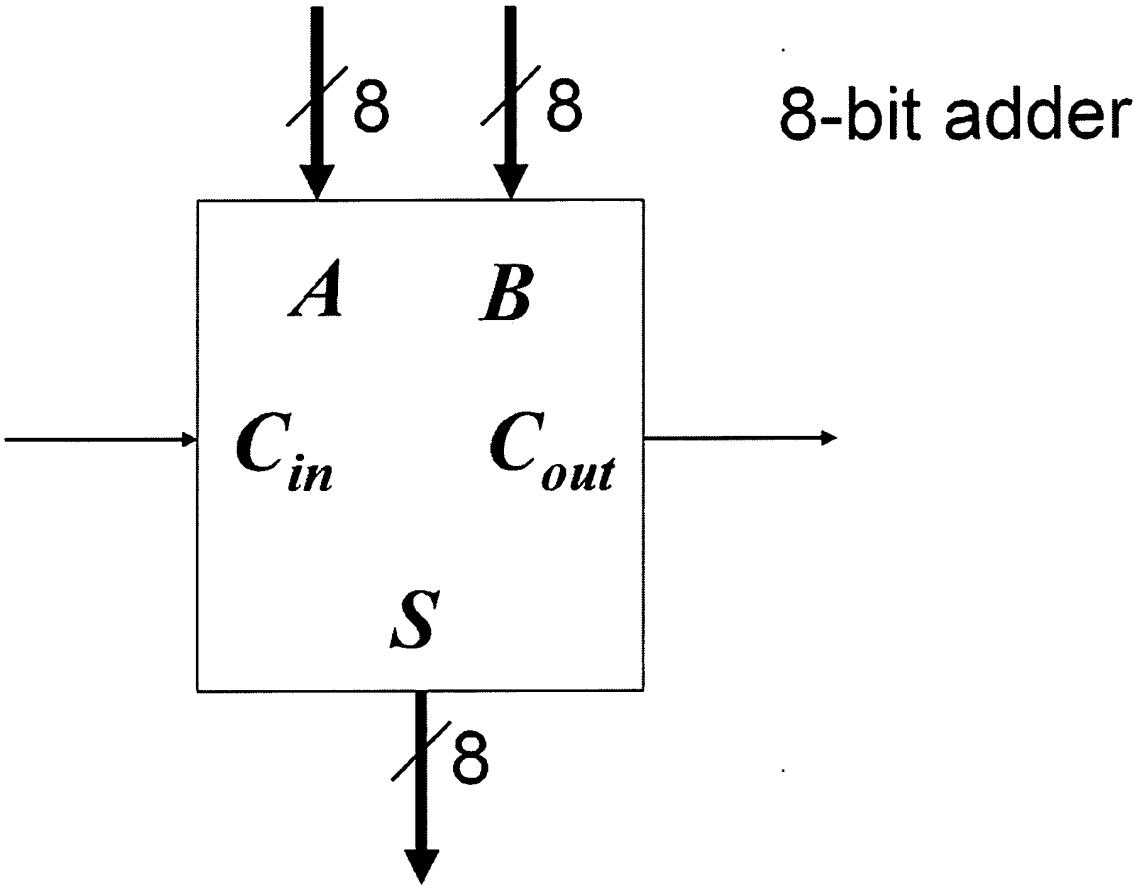


FIG. 11

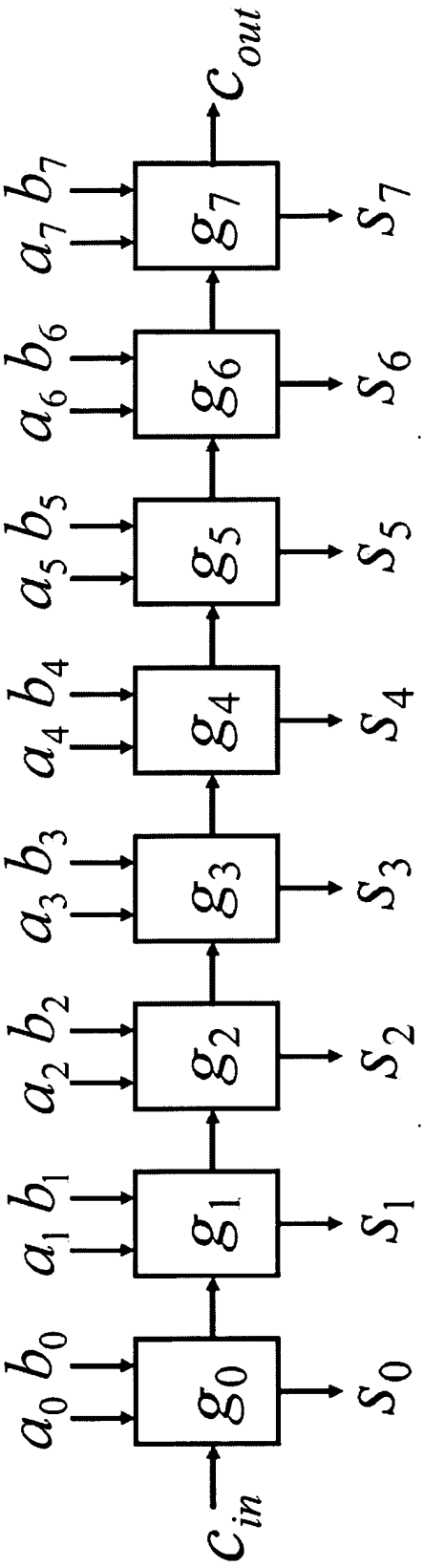

c_{out}
a_7 b_7
g_7
s_7
a_6 b_6
g_6
s_6
a_5 b_5
g_5
s_5
a_4 b_4
g_4
s_4
a_3 b_3
g_3
s_3
a_2 b_2
g_2
s_2
a_1 b_1
g_1
s_1
a_0 b_0
g_0
s_0
c_{in}

FIG. 12

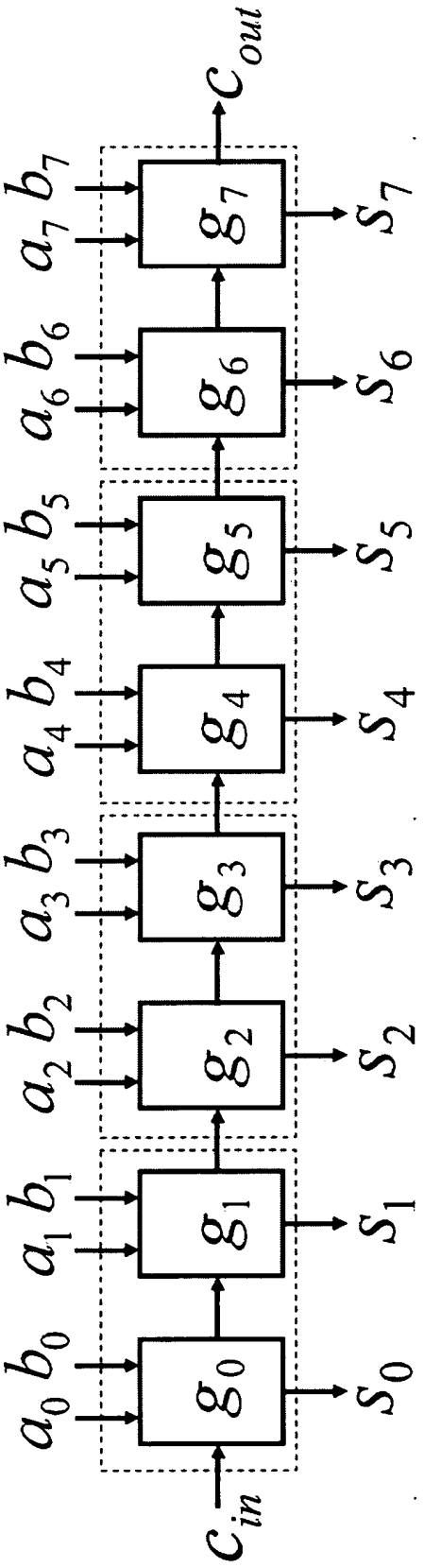

c_{out}
a_7 b_7
g_7
s_7
a_6 b_6
g_6
s_6
a_5 b_5
g_5
s_5
a_4 b_4
g_4
s_4
a_3 b_3
g_3
s_3
a_2 b_2
g_2
s_2
a_1 b_1
g_1
s_1
a_0 b_0
g_0
s_0
c_{in}

FIG. 13

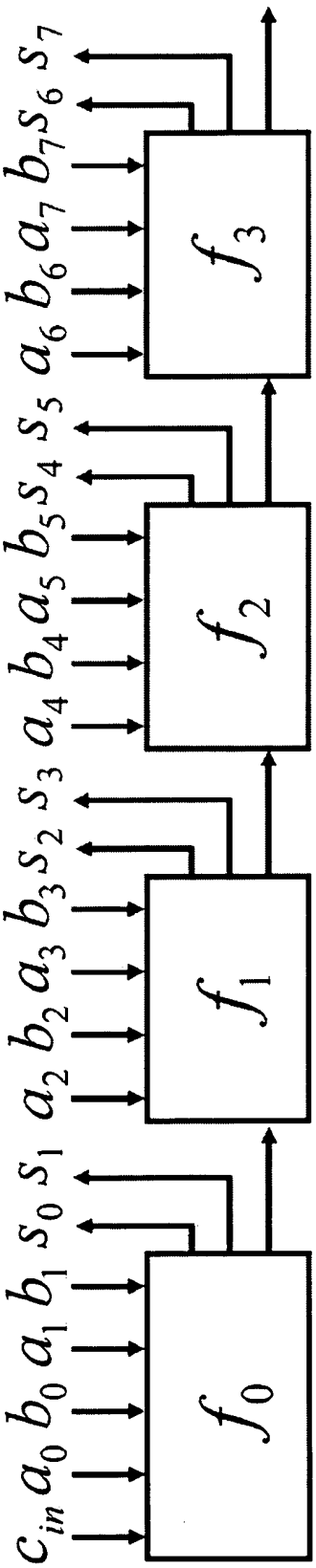

c_{in} a_0 b_0 a_1 b_1 s_0 s_1
f_0
a_2 b_2 a_3 b_3 s_2 s_3
f_1
a_4 b_4 a_5 b_5 s_4 s_5
f_2
a_6 b_6 a_7 b_7 s_6 s_7
f_3

FIG. 14

c_{in}	a_1	a_0	b_1	b_0	c_{out}	s_1	s_0
1	0	0	0	0	0	0	1
1	0	0	0	1	0	1	0
1	0	0	1	0	0	1	1
1	0	0	1	1	1	0	0
1	0	1	0	0	0	1	0
1	0	1	0	1	0	1	1
1	0	1	1	0	1	0	0
1	0	1	1	1	1	0	1
1	1	0	0	0	0	1	1
1	1	0	0	1	1	0	0
1	1	0	1	0	1	0	1
1	1	0	1	1	1	1	0
1	1	1	0	0	1	1	0
1	1	1	0	1	1	1	1
1	1	1	1	0	1	1	1
1	1	1	1	1	1	1	0

c_{in}	a_1	a_0	b_1	b_0	c_{out}	s_1	s_0
0	0	0	0	0	0	0	0
0	0	0	0	1	0	0	1
0	0	0	1	0	0	1	0
0	0	0	1	1	0	1	1
0	0	1	0	0	0	0	1
0	0	1	0	1	0	1	0
0	0	1	1	0	0	1	1
0	0	1	1	1	1	0	0
0	1	0	0	0	0	1	1
0	1	0	0	1	0	1	0
0	1	0	1	0	1	0	0
0	1	0	1	1	1	0	1
0	1	1	0	0	0	1	1
0	1	1	0	1	1	0	0
0	1	1	1	0	1	0	1
0	1	1	1	1	1	1	0

FIG. 15

Address								Memory value							
i_0	i_1	i_2	i_3	i_4	i_5	i_6	i_7	o_7	o_6	o_5	o_4	o_3	o_2	o_1	o_0
0	0	0	0	0	-	-	-	-	-	-	0	0	0	-	-
0	0	0	0	1	-	-	-	-	-	-	0	0	1	-	-
0	0	0	1	0	-	-	-	-	-	-	0	1	0	-	-
0	0	0	1	1	-	-	-	-	-	-	0	1	1	-	-
0	0	1	0	0	-	-	-	-	-	-	0	0	1	-	-
0	0	1	0	1	-	-	-	-	-	-	0	1	0	-	-
0	0	1	1	0	-	-	-	-	-	-	0	1	1	-	-
0	0	1	1	1	-	-	-	-	-	-	1	0	0	-	-
0	1	0	0	0	-	-	-	-	-	-	0	1	0	-	-
0	1	0	0	1	-	-	-	-	-	-	0	1	1	-	-
0	1	0	1	0	-	-	-	-	-	-	1	0	0	-	-
0	1	0	1	1	-	-	-	-	-	-	1	0	1	-	-
0	1	1	0	0	-	-	-	-	-	-	0	1	1	-	-
0	1	1	0	1	-	-	-	-	-	-	1	0	0	-	-
0	1	1	1	0	-	-	-	-	-	-	1	0	1	-	-
0	1	1	1	1	-	-	-	-	-	-	1	1	0	-	-

Address								Memory value							
i_0	i_1	i_2	i_3	i_4	i_5	i_6	i_7	o_7	o_6	o_5	o_4	o_3	o_2	o_1	o_0
1	0	0	0	0	-	-	-	-	-	-	0	0	1	-	-
1	0	0	0	1	-	-	-	-	-	-	0	1	0	-	-
1	0	0	1	0	-	-	-	-	-	-	0	1	1	-	-
1	0	0	1	1	-	-	-	-	-	-	1	0	0	-	-
1	0	1	0	0	-	-	-	-	-	-	0	1	0	-	-
1	0	1	0	1	-	-	-	-	-	-	0	1	1	-	-
1	0	1	1	0	-	-	-	-	-	-	1	0	0	-	-
1	0	1	1	1	-	-	-	-	-	-	1	0	1	-	-
1	1	0	0	0	-	-	-	-	-	-	0	1	1	-	-
1	1	0	0	1	-	-	-	-	-	-	1	0	0	-	-
1	1	0	1	0	-	-	-	-	-	-	1	0	1	-	-
1	1	0	1	1	-	-	-	-	-	-	1	1	0	-	-
1	1	1	0	0	-	-	-	-	-	-	1	0	0	-	-
1	1	1	0	1	-	-	-	-	-	-	1	0	1	-	-
1	1	1	1	0	-	-	-	-	-	-	1	1	0	-	-
1	1	1	1	1	-	-	-	-	-	-	1	1	1	-	-

FIG. 16

Address								Memory value							
i_0	i_1	i_2	i_3	i_4	i_5	i_6	i_7	o_7	o_6	o_5	o_4	o_3	o_2	o_1	o_0
0	-	-	-	0	0	0	0	-	-	-	0	0	0	-	-
0	-	-	-	0	0	0	1	-	-	-	0	0	1	-	-
0	-	-	-	0	0	1	0	-	-	-	0	1	0	-	-
0	-	-	-	0	0	1	1	-	-	-	0	1	1	-	-
0	-	-	-	0	1	0	0	-	-	-	0	0	1	-	-
0	-	-	-	0	1	0	1	-	-	-	0	1	0	-	-
0	-	-	-	0	1	1	0	-	-	-	0	1	1	-	-
0	-	-	-	0	1	1	1	-	-	-	1	0	0	-	-
0	-	-	-	1	0	0	0	-	-	-	0	1	0	-	-
0	-	-	-	1	0	0	1	-	-	-	0	1	1	-	-
0	-	-	-	1	0	1	0	-	-	-	1	0	0	-	-
0	-	-	-	1	0	1	1	-	-	-	1	0	1	-	-
0	-	-	-	1	1	0	0	-	-	-	0	1	1	-	-
0	-	-	-	1	1	0	1	-	-	-	1	0	0	-	-
0	-	-	-	1	1	1	0	-	-	-	1	0	1	-	-
0	-	-	-	1	1	1	1	-	-	-	1	1	0	-	-

Address								Memory value							
i_0	i_1	i_2	i_3	i_4	i_5	i_6	i_7	o_7	o_6	o_5	o_4	o_3	o_2	o_1	o_0
1	-	-	-	0	0	0	0	-	-	-	0	0	1	-	-
1	-	-	-	0	0	0	1	-	-	-	0	1	0	-	-
1	-	-	-	0	0	1	0	-	-	-	0	1	1	-	-
1	-	-	-	0	0	1	1	-	-	-	1	0	0	-	-
1	-	-	-	0	1	0	0	-	-	-	0	1	0	-	-
1	-	-	-	0	1	0	1	-	-	-	0	1	1	-	-
1	-	-	-	0	1	1	0	-	-	-	1	0	0	-	-
1	-	-	-	0	1	1	1	-	-	-	1	0	1	-	-
1	-	-	-	1	0	0	0	-	-	-	0	1	1	-	-
1	-	-	-	1	0	0	1	-	-	-	1	0	0	-	-
1	-	-	-	1	0	1	0	-	-	-	1	0	1	-	-
1	-	-	-	1	0	1	1	-	-	-	1	1	0	-	-
1	-	-	-	1	1	0	0	-	-	-	1	0	0	-	-
1	-	-	-	1	1	0	1	-	-	-	1	0	1	-	-
1	-	-	-	1	1	1	0	-	-	-	1	1	0	-	-
1	-	-	-	1	1	1	1	-	-	-	1	1	1	-	-

FIG. 17

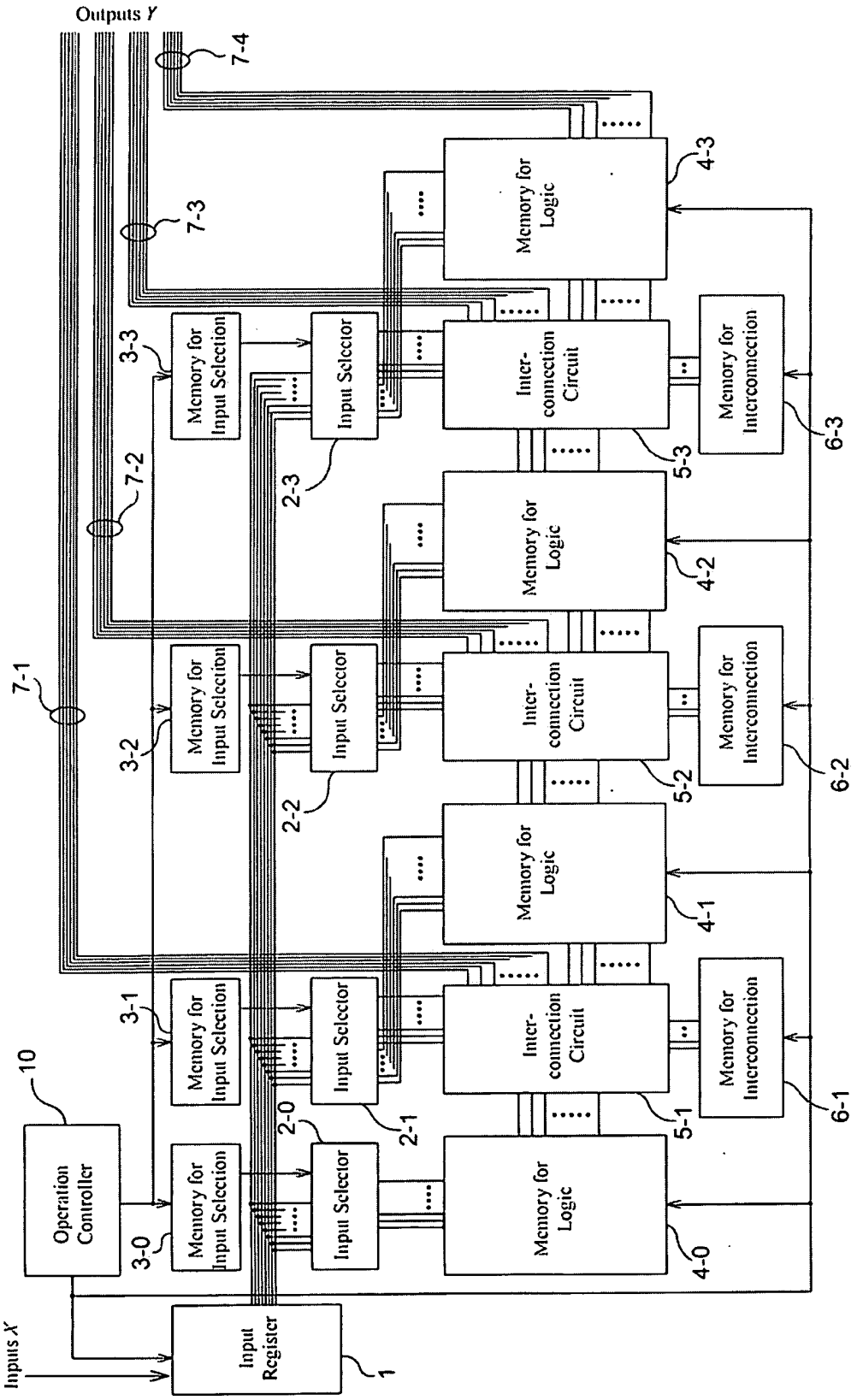

Outputs Y
7-4
7-3
7-2
7-1
Memory for Logic
4-3
Memory for Input Selection
3-3
Input Selector
2-3
Inter-connection Circuit
5-3
Memory for Interconnection
6-3
Memory for Logic
4-2
Memory for Input Selection
3-2
Input Selector
2-2
Inter-connection Circuit
5-2
Memory for Interconnection
6-2
Memory for Logic
4-1
Memory for Input Selection
3-1
Input Selector
2-1
Inter-connection Circuit
5-1
Memory for Interconnection
6-1
Operation Controller
10
Memory for Input Selection
3-0
Input Selector
2-0
Memory for Logic
4-0
Inputs X
Input Register
1

FIG. 18

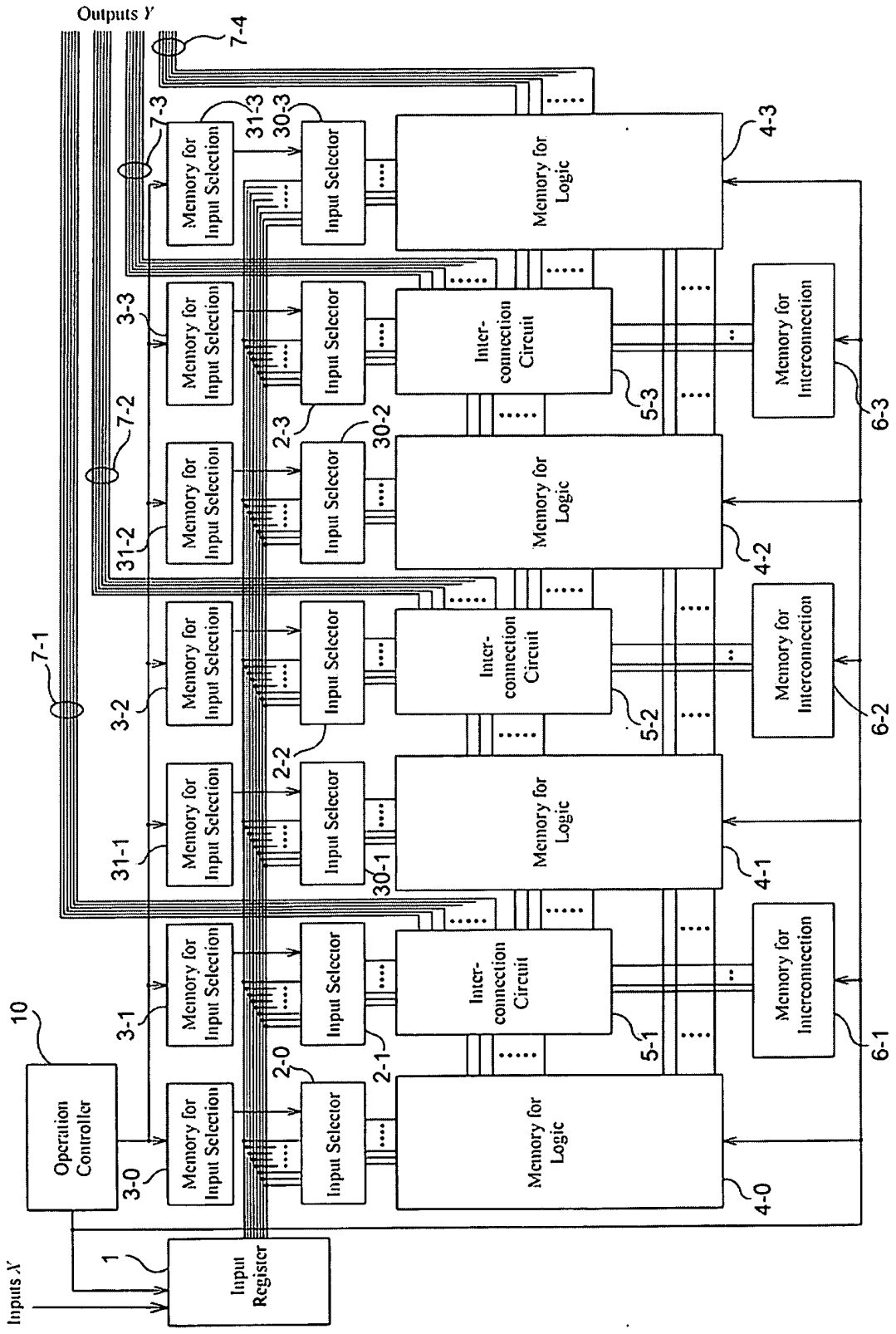

Outputs Y
7-4
7-3
7-2
7-1
Memory for Input Selection
Input Selector
Memory for Logic
Inter-connection Circuit
Memory for Interconnection
Operation Controller
10
Input Register
1
Inputs X
3-3
3-2
3-1
3-0
2-3
2-2
2-1
2-0
31-3
31-2
31-1
30-3
30-2
30-1
4-3
4-2
4-1
4-0
5-3
5-2
5-1
6-3
6-2
6-1

FIG. 19

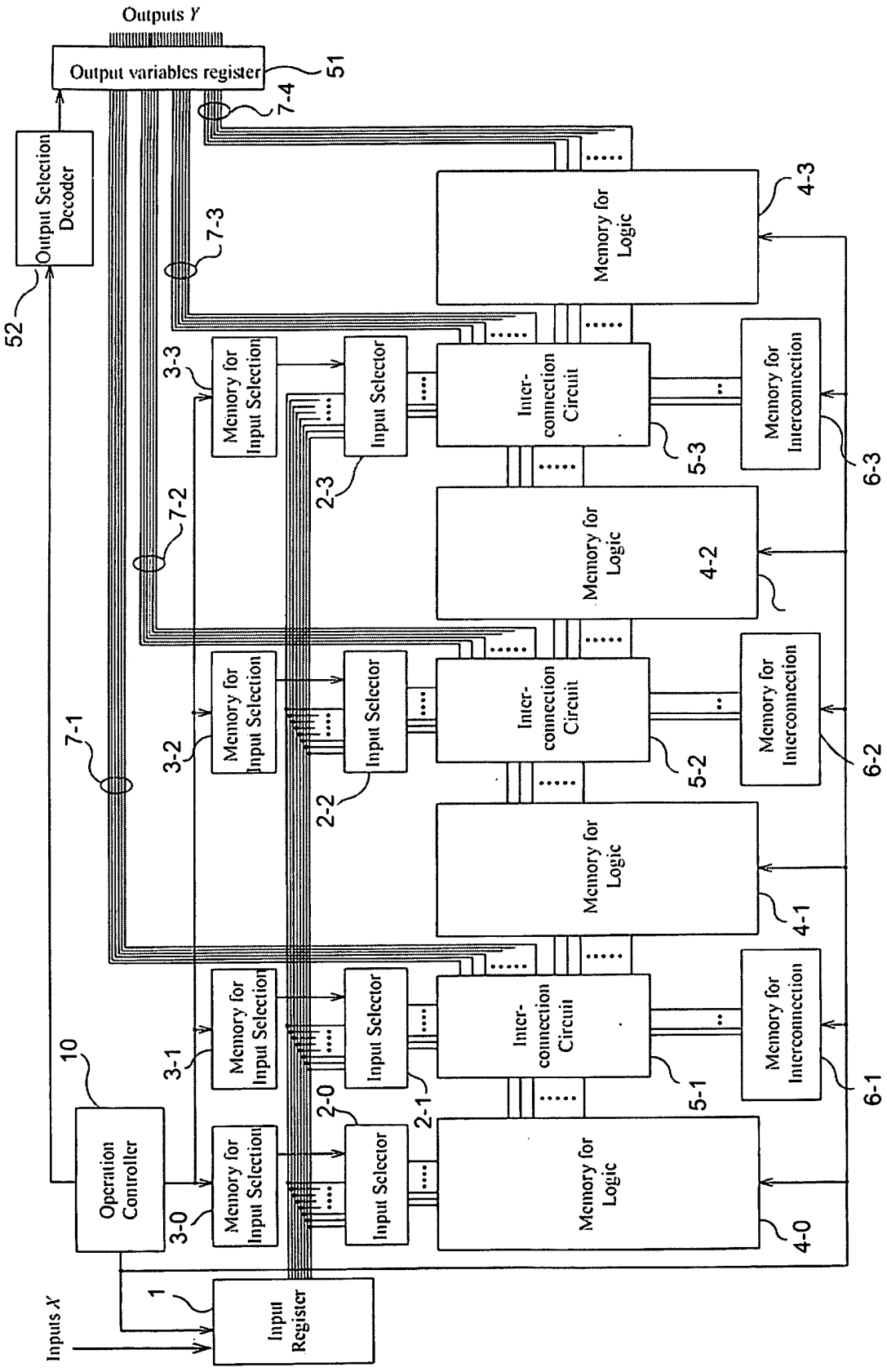

Outputs Y
Output variables register
51
7-4
Output Selection Decoder
52
7-3
Memory for Logic
4-3
3-3
Memory for Input Selection
Input Selector
2-3
Inter-connection Circuit
5-3
Memory for Interconnection
6-3
7-2
Memory for Logic
4-2
3-2
Memory for Input Selection
Input Selector
2-2
Inter-connection Circuit
5-2
Memory for Interconnection
6-2
7-1
Memory for Logic
4-1
3-1
Memory for Input Selection
Input Selector
2-1
Inter-connection Circuit
5-1
Memory for Interconnection
6-1
10
Operation Controller
3-0
Memory for Input Selection
Input Selector
2-0
Memory for Logic
4-0
1
Input Register
Inputs X

FIG. 20

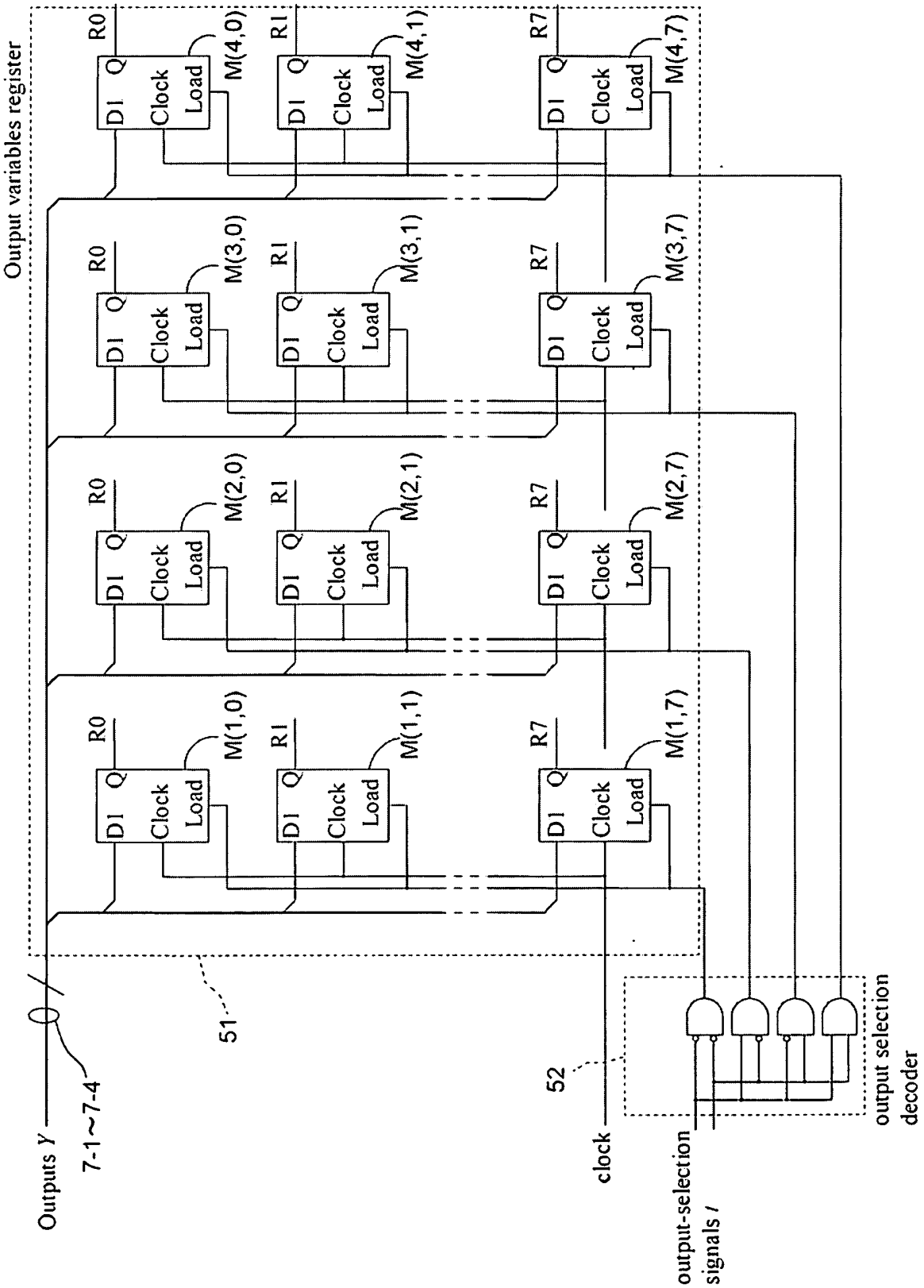

Output variables register
R0
R1
R7
D1
Q
Clock
Load
M(4,0)
M(4,1)
M(4,7)
M(3,0)
M(3,1)
M(3,7)
M(2,0)
M(2,1)
M(2,7)
M(1,0)
M(1,1)
M(1,7)
51
52
Outputs Y
7-1~7-4
clock
output-selection signals I
output selection decoder

FIG. 21

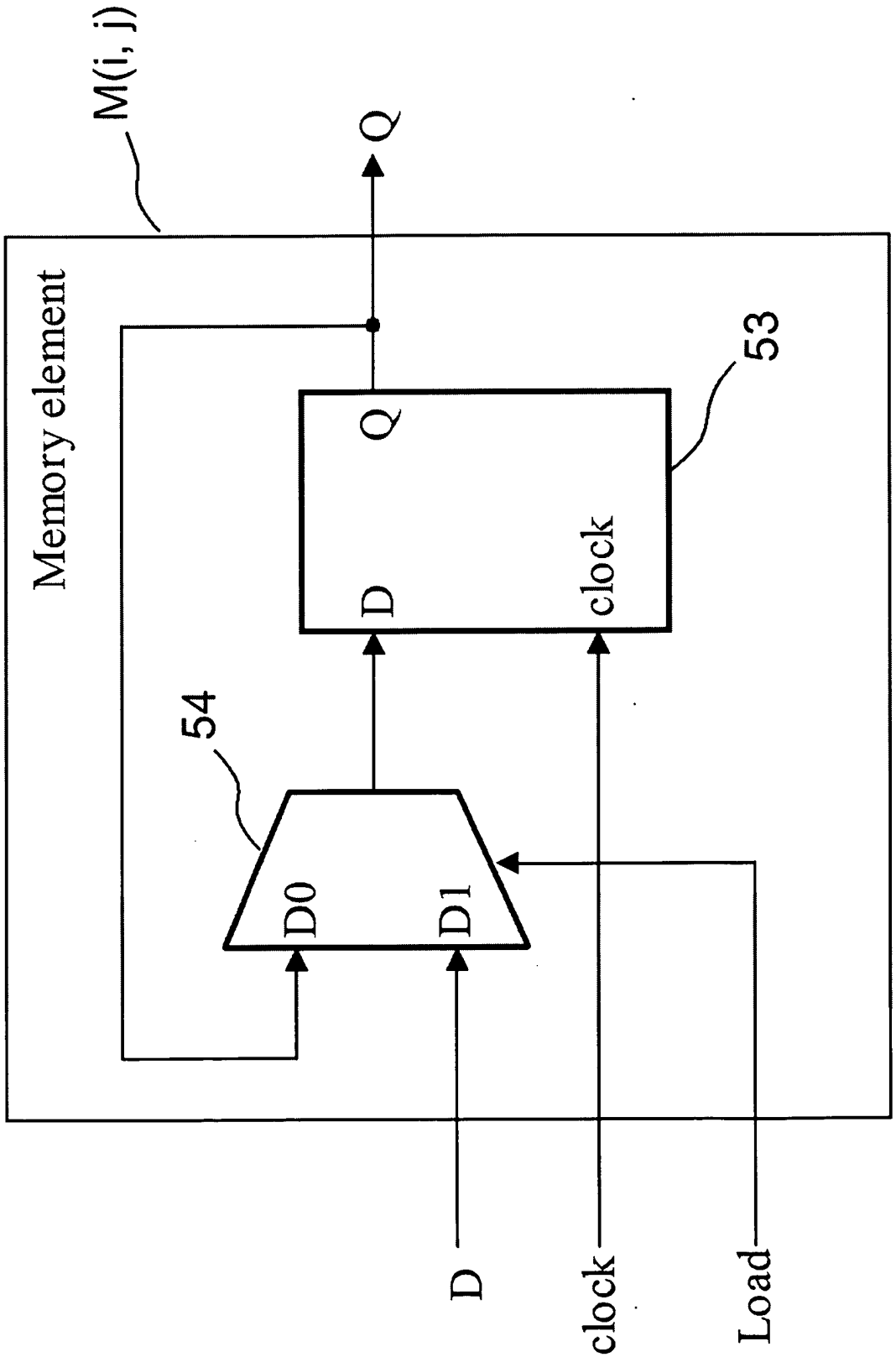


FIG. 22

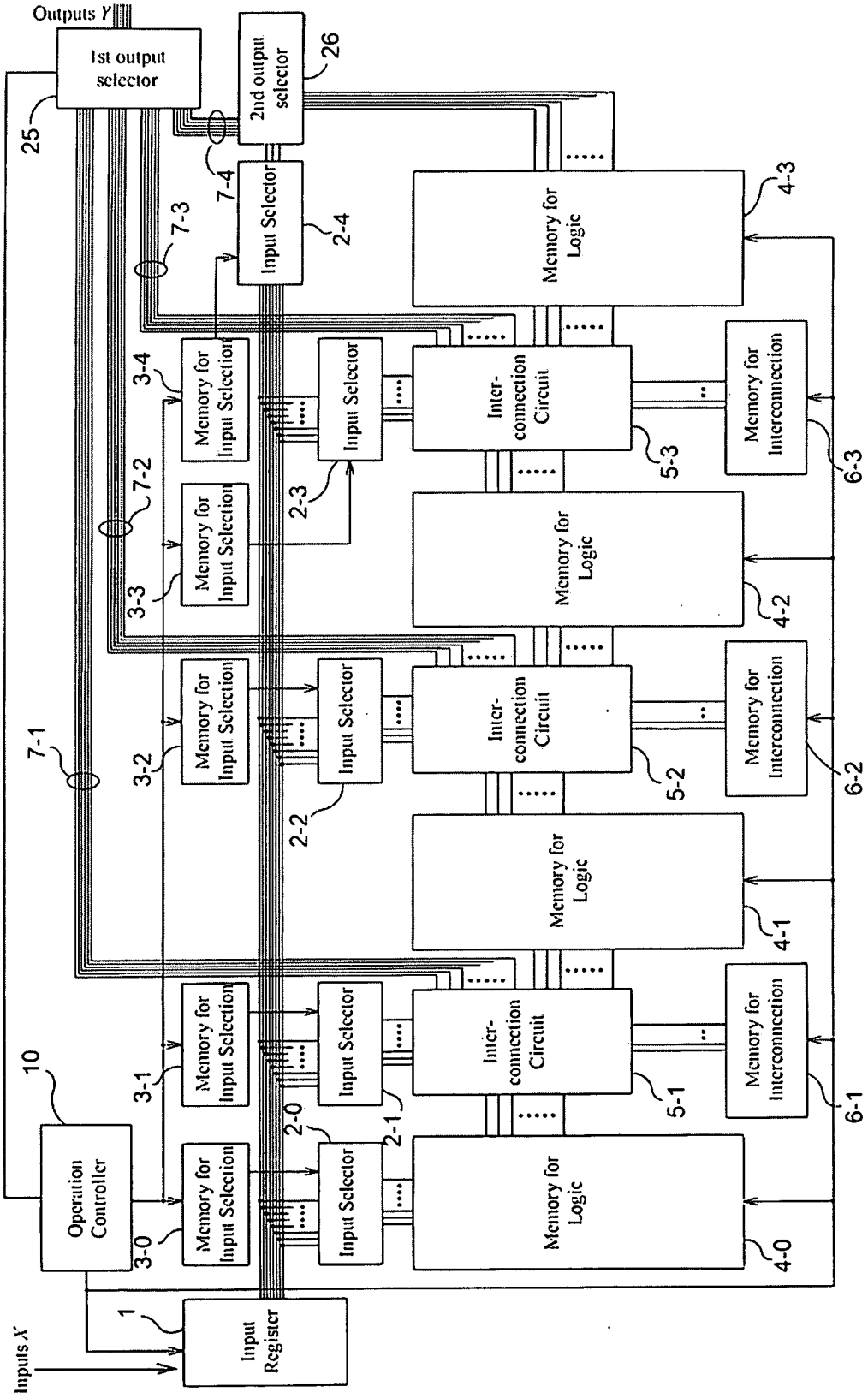

Outputs Y
1st output selector
2nd output selector
26
25
7-4
7-3
Input Selector
2-4
Memory for Logic
4-3
Memory for Input Selection
3-4
Input Selector
Inter-connection Circuit
Memory for Interconnection
5-3
6-3
7-2
2-3
Memory for Logic
4-2
3-3
Memory for Input Selection
Input Selector
Inter-connection Circuit
Memory for Interconnection
7-1
3-2
5-2
6-2
2-2
Memory for Logic
4-1
Memory for Input Selection
Input Selector
Inter-connection Circuit
Memory for Interconnection
10
3-1
5-1
6-1
2-0
2-1
Operation Controller
Memory for Input Selection
Input Selector
Memory for Logic
4-0
3-0
1
Input Register
Inputs X

FIG. 23

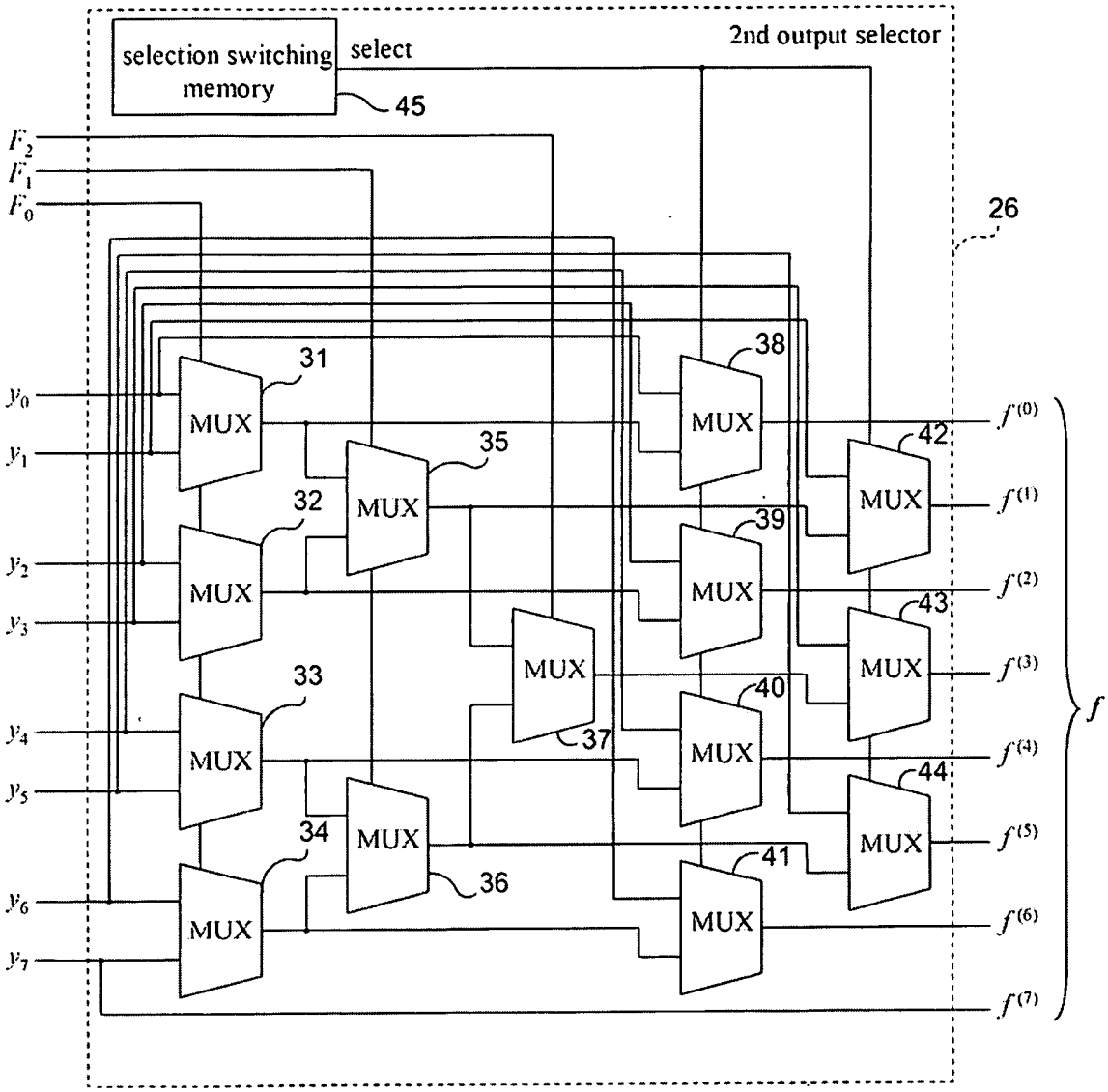

selection switching memory
select
45
2nd output selector
26
F_2
F_1
F_0
y_0
y_1
y_2
y_3
y_4
y_5
y_6
y_7
MUX
31
32
33
34
35
36
37
38
39
40
41
42
43
44
$f^{(0)}$
$f^{(1)}$
$f^{(2)}$
$f^{(3)}$
$f^{(4)}$
$f^{(5)}$
$f^{(6)}$
$f^{(7)}$
f

FIG. 24

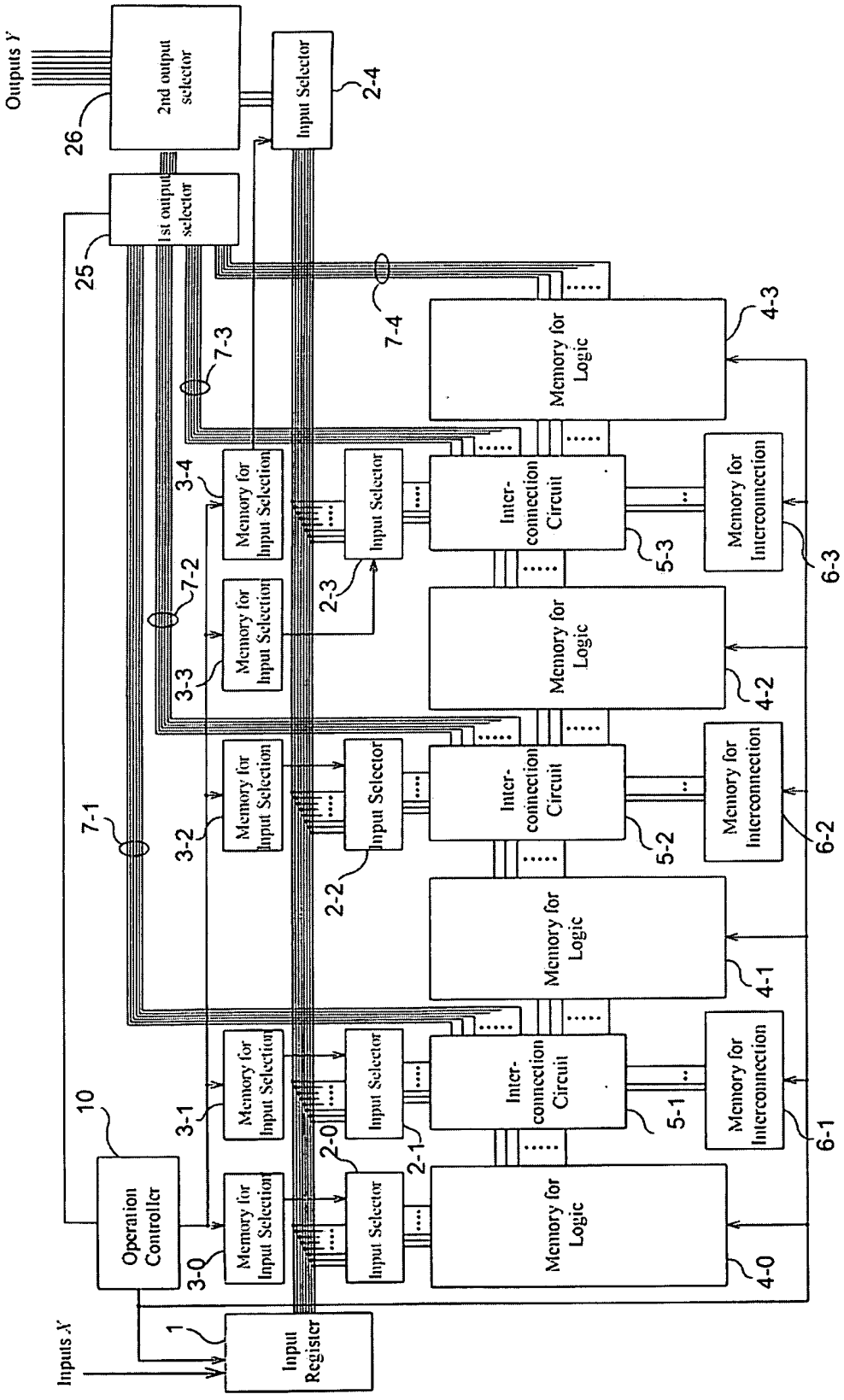

Outputs Y
2nd output selector
26
Input Selector
2-4
1st output selector
25
7-4
7-3
Memory for Logic
4-3
Memory for Input Selection
3-4
Input Selector
Inter-connection Circuit
5-3
Memory for Interconnection
6-3
7-2
2-3
3-3
Memory for Logic
4-2
7-1
3-2
2-2
5-2
6-2
Memory for Logic
4-1
10
3-1
2-0
2-1
5-1
6-1
Operation Controller
3-0
Memory for Logic
4-0
Inputs X
1
Input Register

FIG. 25

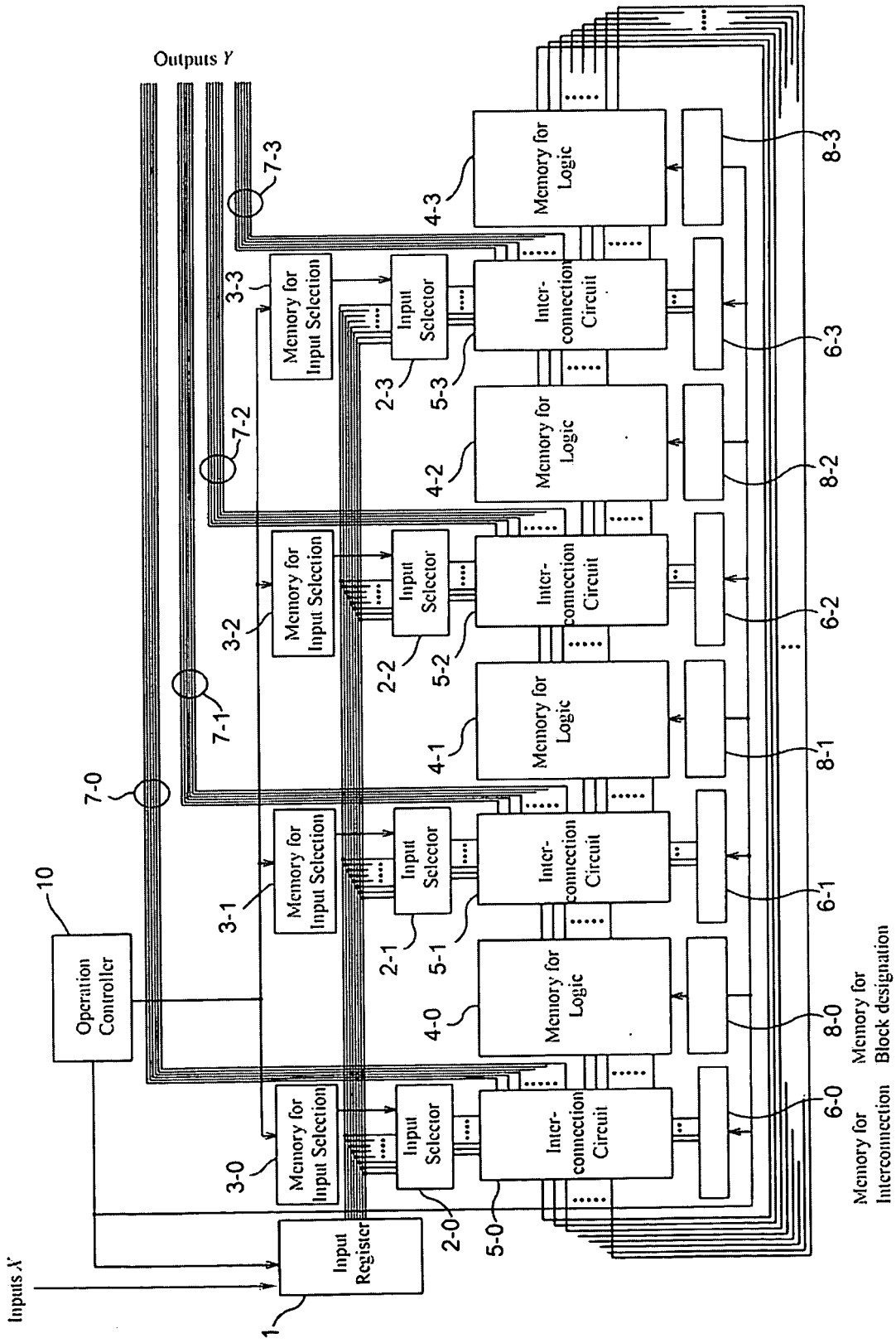

Outputs Y
Inputs X
Operation Controller
Input Register
Memory for Input Selection
Input Selector
Inter-connection Circuit
Memory for Logic
Memory for Interconnection
Memory for Block designation

FIG. 26

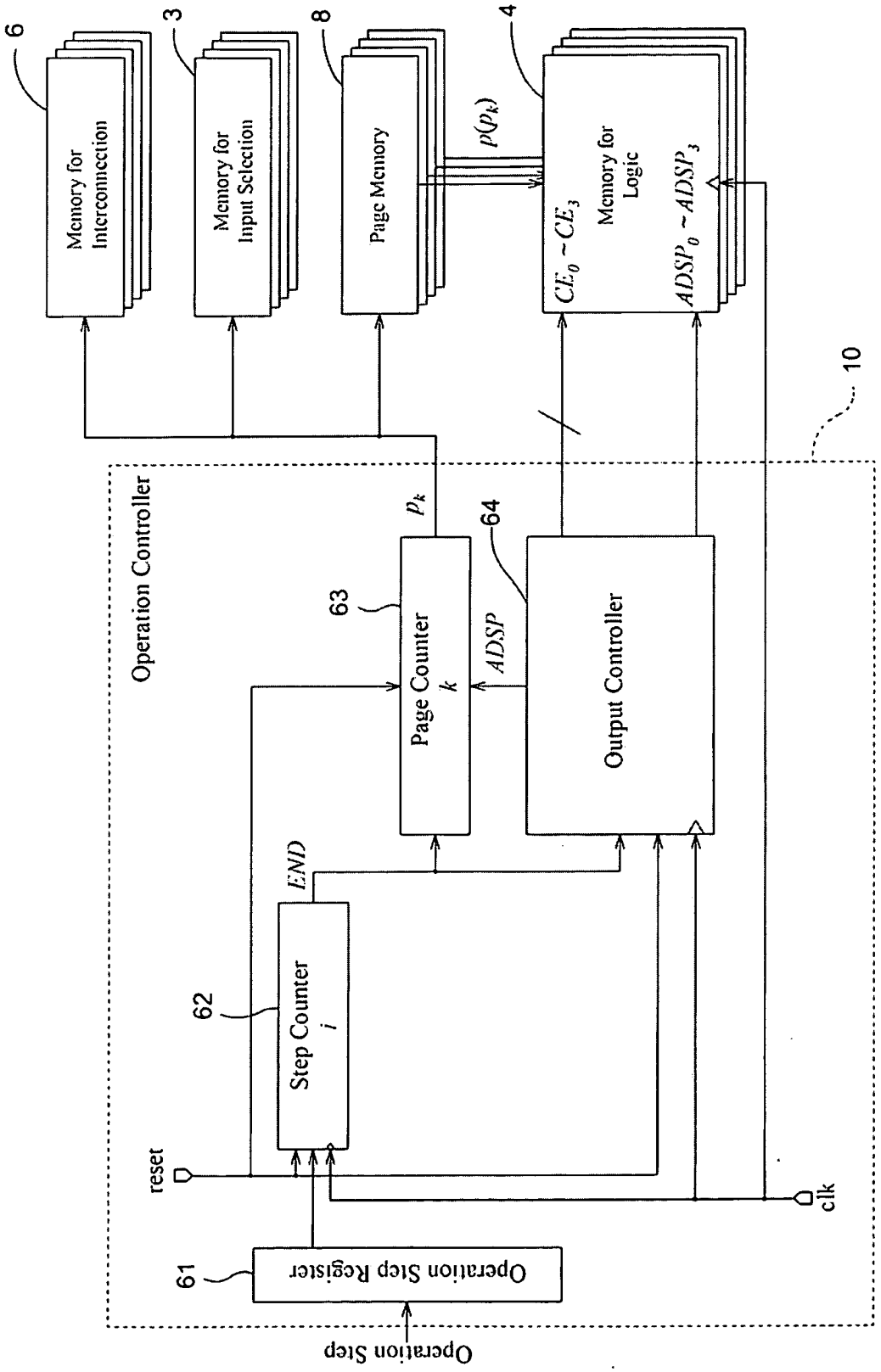

6
Memory for Interconnection
3
Memory for Input Selection
8
Page Memory
$p(p_k)$
4
Memory for Logic
$CE_0 \sim CE_3$
$ADSP_0 \sim ADSP_3$
10
Operation Controller
p_k
64
63
Page Counter
k
$ADSP$
Output Controller
END
62
Step Counter
i
reset
clk
61
Operation Step Register
Operation Step

FIG. 27

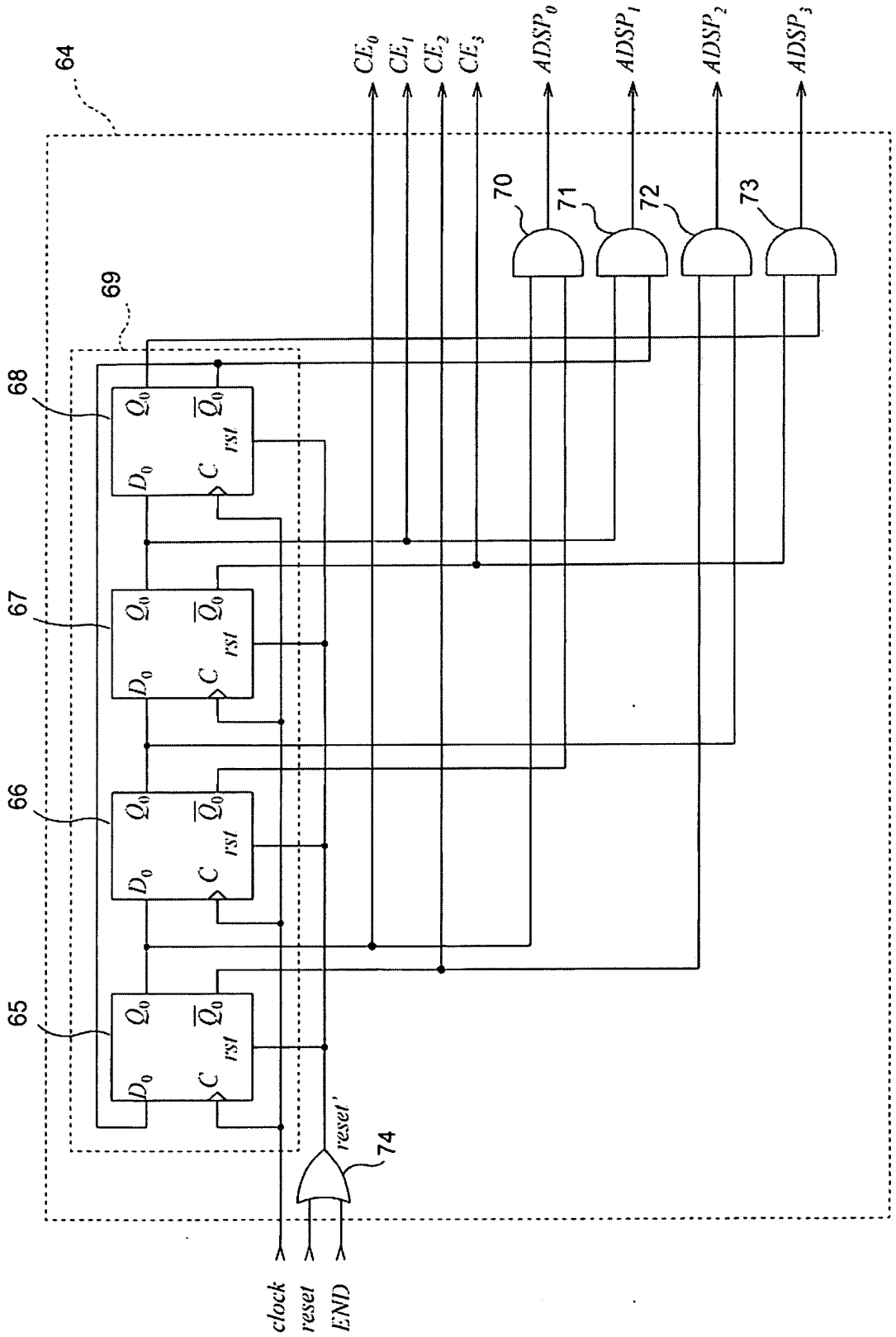

64
69
68
67
66
65
70
71
72
73
74
CE_0
CE_1
CE_2
CE_3
$ADSP_0$
$ADSP_1$
$ADSP_2$
$ADSP_3$
Q_0
$\overline{Q}_0$
D_0
C
rst
reset'
clock
reset
END

FIG. 28a

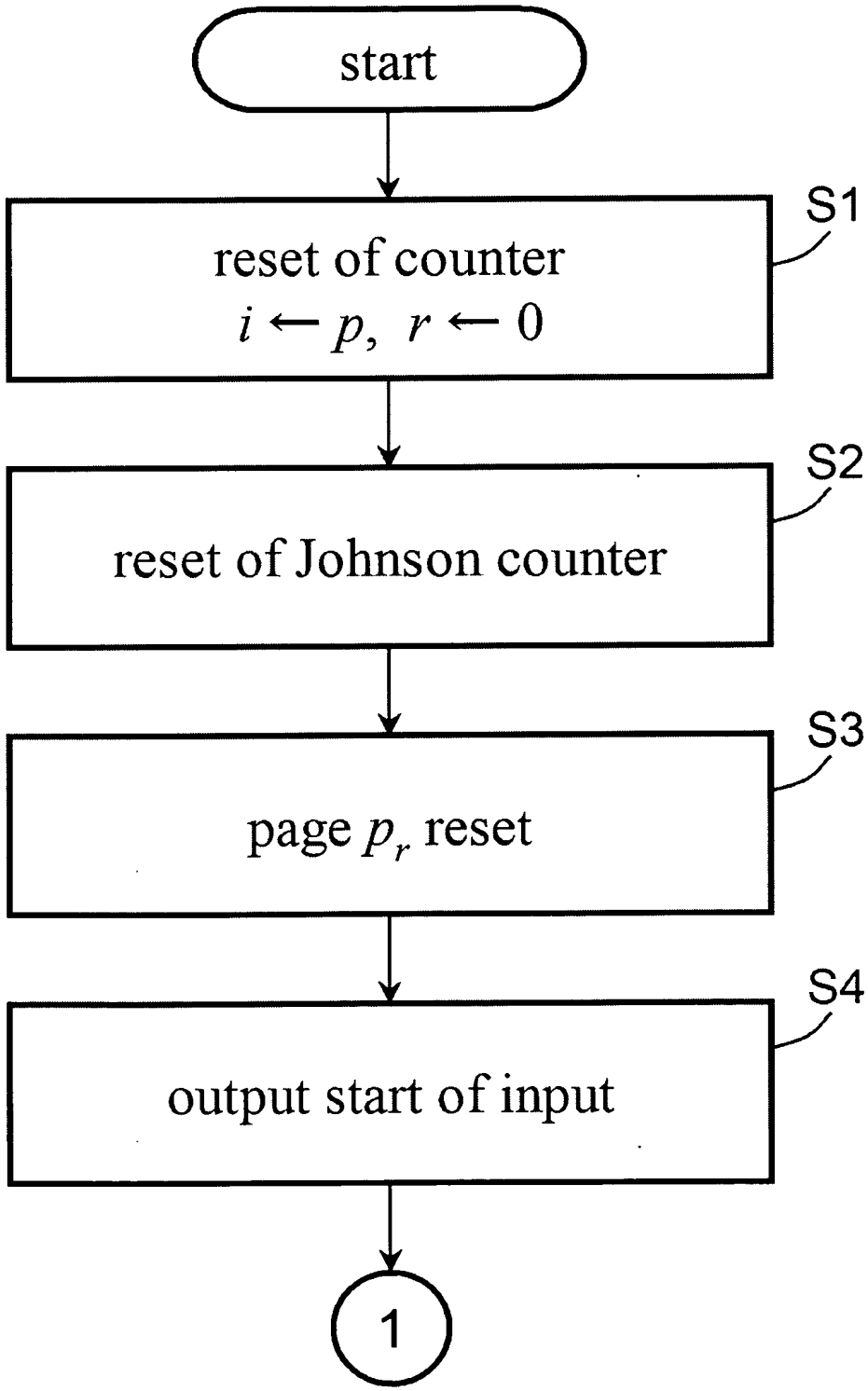

start
reset of counter
$i \leftarrow p,\ r \leftarrow 0$
S1
reset of Johnson counter
S2
page p_r reset
S3
output start of input
S4
1

FIG. 28b

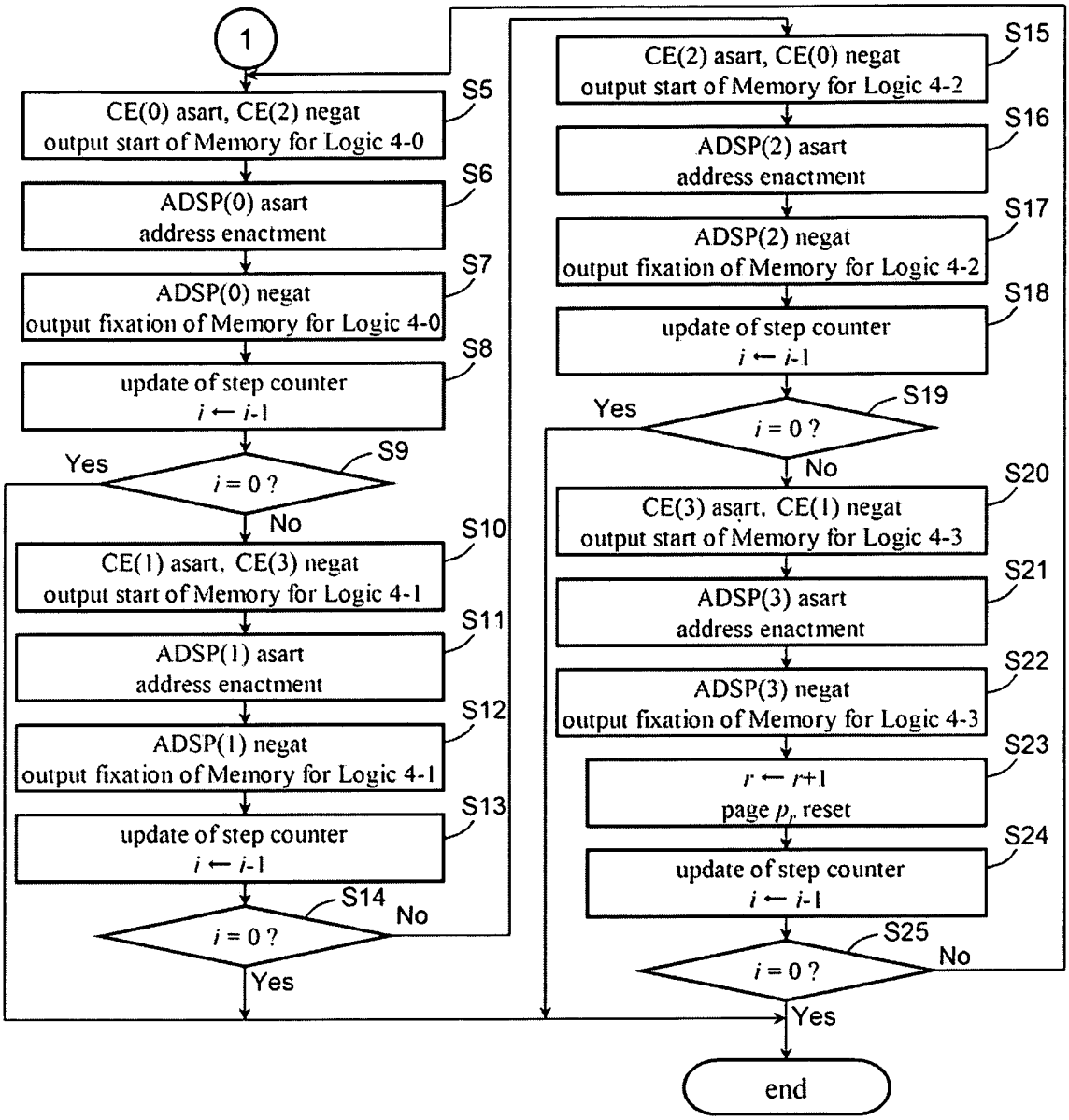

1
CE(0) asart, CE(2) negat
output start of Memory for Logic 4-0
S5
ADSP(0) asart
address enactment
S6
ADSP(0) negat
output fixation of Memory for Logic 4-0
S7
update of step counter
i ← i-1
S8
Yes
i = 0 ?
S9
No
CE(1) asart, CE(3) negat
output start of Memory for Logic 4-1
S10
ADSP(1) asart
address enactment
S11
ADSP(1) negat
output fixation of Memory for Logic 4-1
S12
update of step counter
i ← i-1
S13
i = 0 ?
S14
No
Yes
CE(2) asart, CE(0) negat
output start of Memory for Logic 4-2
S15
ADSP(2) asart
address enactment
S16
ADSP(2) negat
output fixation of Memory for Logic 4-2
S17
update of step counter
i ← i-1
S18
Yes
i = 0 ?
S19
No
CE(3) asart, CE(1) negat
output start of Memory for Logic 4-3
S20
ADSP(3) asart
address enactment
S21
ADSP(3) negat
output fixation of Memory for Logic 4-3
S22
r ← r+1
page p_r reset
S23
update of step counter
i ← i-1
S24
i = 0 ?
S25
No
Yes
end

FIG. 29

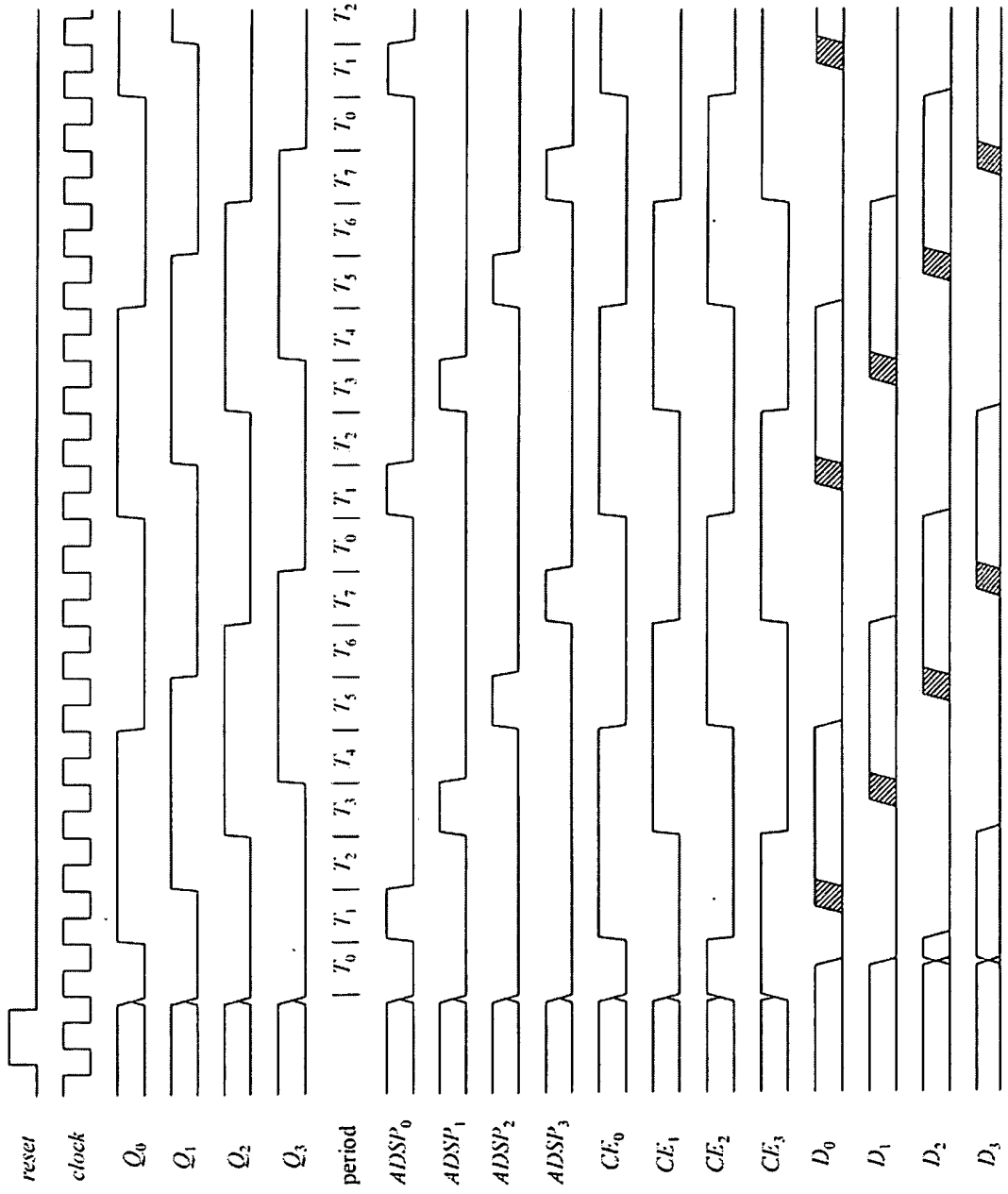

reset
clock
Q_0
Q_1
Q_2
Q_3
period
$ADSP_0$
$ADSP_1$
$ADSP_2$
$ADSP_3$
CE_0
CE_1
CE_2
CE_3
D_0
D_1
D_2
D_3
| T_0 | T_1 | T_2 | T_3 | T_4 | T_5 | T_6 | T_7 | T_0 | T_1 | T_2 | T_3 | T_4 | T_5 | T_6 | T_7 | T_0 | T_1 | T_2

FIG. 30

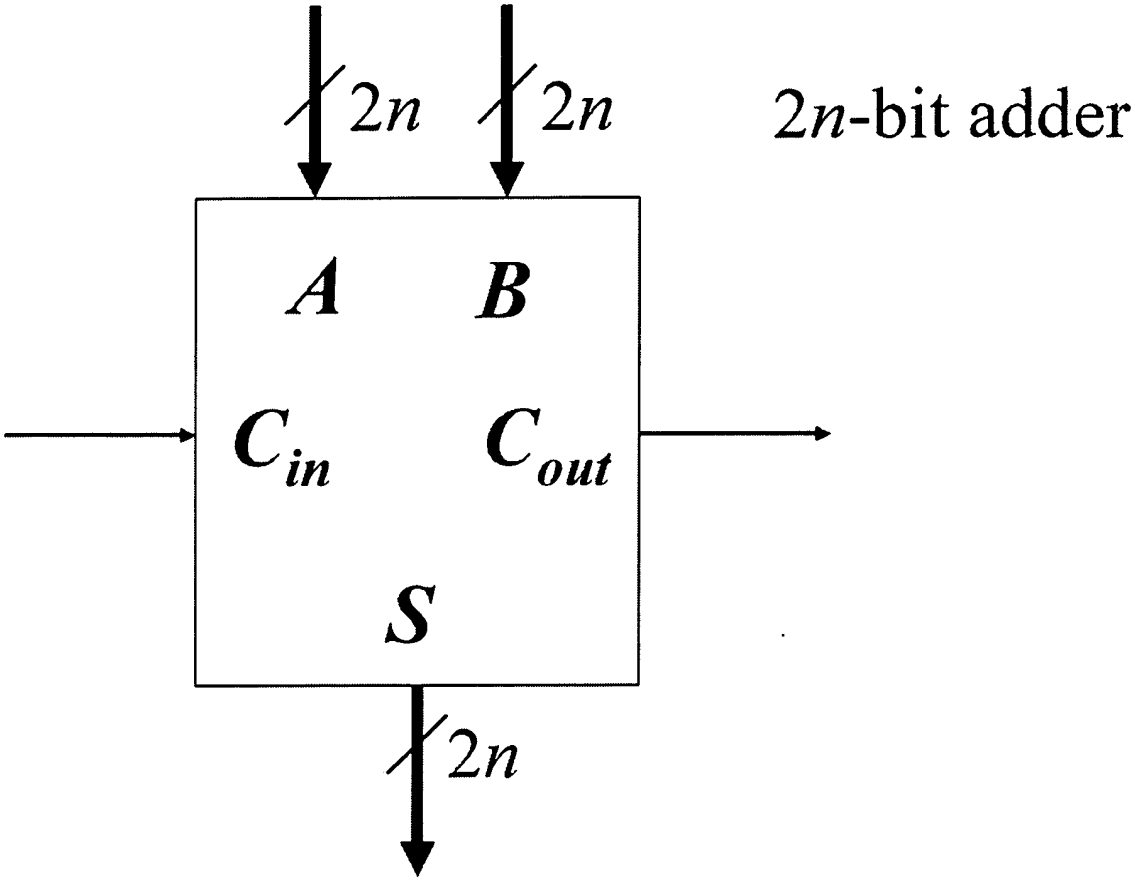


FIG. 31

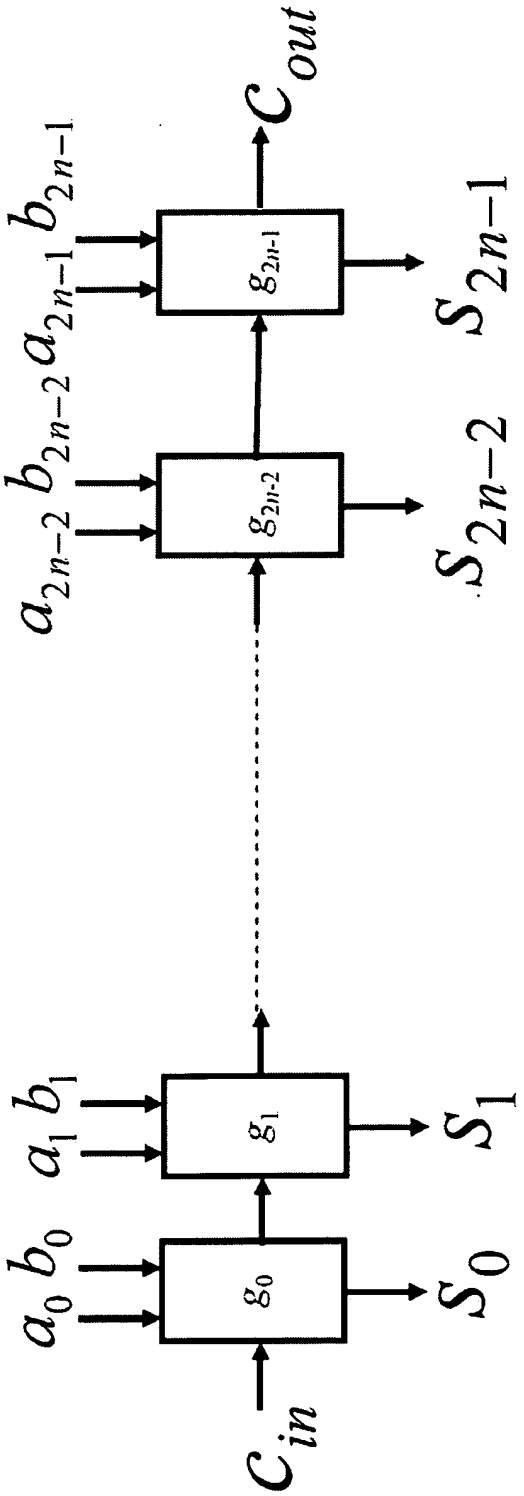

c_{out}
a_{2n-1} b_{2n-1}
g_{2n-1}
s_{2n-1}
a_{2n-2} b_{2n-2}
g_{2n-2}
s_{2n-2}
a_1 b_1
g_1
s_1
a_0 b_0
g_0
s_0
c_{in}

FIG. 32

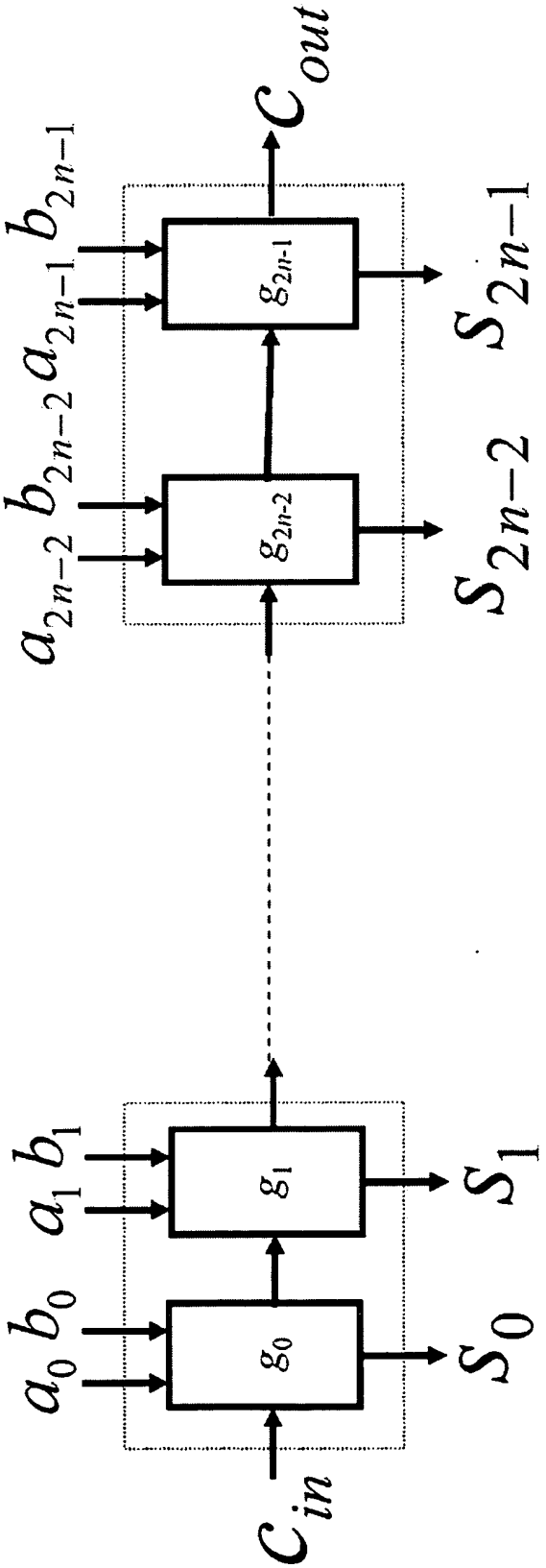

c_{out}
b_{2n-1}
a_{2n-1}
g_{2n-1}
s_{2n-1}
b_{2n-2}
a_{2n-2}
g_{2n-2}
s_{2n-2}
b_1
a_1
g_1
s_1
b_0
a_0
g_0
s_0
c_{in}

FIG. 33

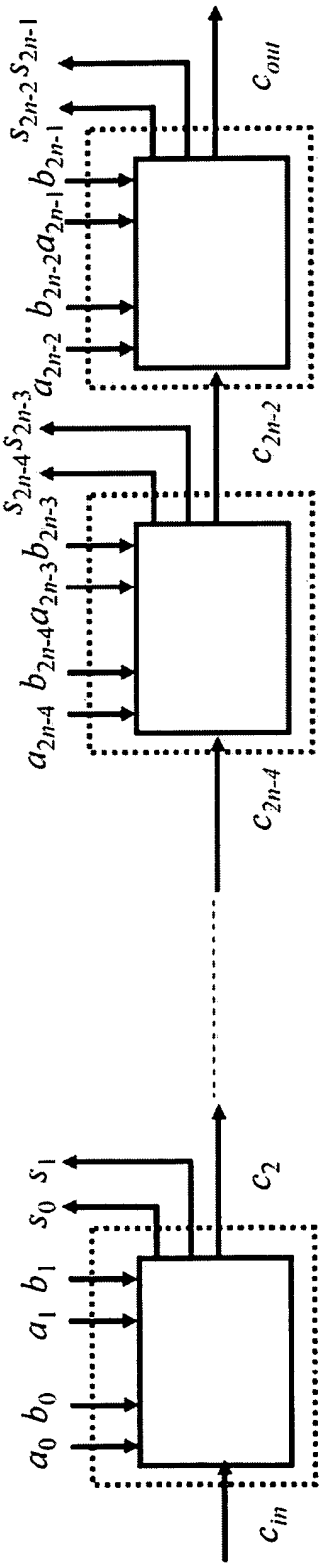

s_{2n-2} s_{2n-1}
c_{out}
b_{2n-1}
a_{2n-1}
b_{2n-2}
a_{2n-2}
s_{2n-4} s_{2n-3}
c_{2n-2}
b_{2n-3}
a_{2n-3}
b_{2n-4}
a_{2n-4}
c_{2n-4}
s_1
s_0
c_2
b_1
a_1
b_0
a_0
c_{in}

FIG. 34

c_{in}	a_1	a_0	b_1	b_0	c_{out}	s_1	s_0
0	0	0	0	0	0	0	0
0	0	0	0	1	0	0	1
0	0	0	1	0	0	1	0
0	0	0	1	1	0	1	1
0	0	1	0	0	0	1	1
0	0	1	0	1	0	1	0
0	0	1	1	0	0	0	1
0	0	1	1	1	1	0	0
0	1	0	0	0	0	1	0
0	1	0	0	1	0	1	1
0	1	0	1	0	1	0	0
0	1	0	1	1	1	0	1
0	1	1	0	0	0	1	1
0	1	1	0	1	1	1	0
0	1	1	1	0	1	1	1
0	1	1	1	1	1	1	0
1	0	0	0	0	0	0	1
1	0	0	0	1	0	0	0
1	0	0	1	0	0	1	1
1	0	0	1	1	1	1	0
1	0	1	0	0	0	1	0
1	0	1	0	1	0	1	1
1	0	1	1	0	1	0	0
1	0	1	1	1	1	0	1
1	1	0	0	0	0	1	0
1	1	0	0	1	0	1	1
1	1	0	1	0	1	0	0
1	1	0	1	1	1	0	1
1	1	1	0	0	1	1	0
1	1	1	0	1	1	1	1
1	1	1	1	0	1	1	1
1	1	1	1	1	1	1	0

FIG. 35

address								output value							
i_0	i_1	i_2	i_3	i_4	i_5	i_6	i_7	o_7	o_6	o_5	o_4	o_3	o_2	o_1	o_0
0	0	0	0	0	—	—	—	—	—	—	0	0	0	—	—
0	0	0	0	1	—	—	—	—	—	—	0	1	1	—	—
0	0	0	1	0	—	—	—	—	—	—	0	1	0	—	—
0	0	0	1	1	—	—	—	—	—	—	0	1	1	—	—
0	0	1	0	0	—	—	—	—	—	—	1	0	0	—	—
0	0	1	0	1	—	—	—	—	—	—	1	0	1	—	—
0	0	1	1	0	—	—	—	—	—	—	1	1	0	—	—
0	0	1	1	1	—	—	—	—	—	—	1	1	1	—	—
0	1	0	0	0	—	—	—	—	—	—	0	0	0	—	—
0	1	0	0	1	—	—	—	—	—	—	0	0	1	—	—
0	1	0	1	0	—	—	—	—	—	—	0	1	0	—	—
0	1	0	1	1	—	—	—	—	—	—	0	1	1	—	—
0	1	1	0	0	—	—	—	—	—	—	1	0	0	—	—
0	1	1	0	1	—	—	—	—	—	—	1	0	1	—	—
0	1	1	1	0	—	—	—	—	—	—	1	1	0	—	—
0	1	1	1	1	—	—	—	—	—	—	1	1	1	—	—

address								output value							
i_0	i_1	i_2	i_3	i_4	i_5	i_6	i_7	o_7	o_6	o_5	o_4	o_3	o_2	o_1	o_0
1	0	0	0	0	—	—	—	—	—	—	0	0	1	—	—
1	0	0	0	1	—	—	—	—	—	—	0	1	0	—	—
1	0	0	1	0	—	—	—	—	—	—	0	1	1	—	—
1	0	0	1	1	—	—	—	—	—	—	1	0	0	—	—
1	0	1	0	0	—	—	—	—	—	—	1	0	1	—	—
1	0	1	0	1	—	—	—	—	—	—	1	1	0	—	—
1	0	1	1	0	—	—	—	—	—	—	1	1	1	—	—
1	0	1	1	1	—	—	—	—	—	—	0	0	0	—	—
1	1	0	0	0	—	—	—	—	—	—	0	0	1	—	—
1	1	0	0	1	—	—	—	—	—	—	0	1	0	—	—
1	1	0	1	0	—	—	—	—	—	—	0	1	1	—	—
1	1	0	1	1	—	—	—	—	—	—	1	0	0	—	—
1	1	1	0	0	—	—	—	—	—	—	1	0	1	—	—
1	1	1	0	1	—	—	—	—	—	—	1	1	0	—	—
1	1	1	1	0	—	—	—	—	—	—	1	1	1	—	—
1	1	1	1	1	—	—	—	—	—	—	1	1	1	—	—

FIG. 36

address								output value							
i_0	i_1	i_2	i_3	i_4	i_5	i_6	i_7	o_7	o_6	o_5	o_4	o_3	o_2	o_1	o_0
0	–	–	–	0	0	0	0	–	–	–	0	0	0	–	–
0	–	–	–	0	0	0	1	–	–	–	0	0	1	–	–
0	–	–	–	0	0	1	0	–	–	–	0	1	0	–	–
0	–	–	–	0	0	1	1	–	–	–	0	1	1	–	–
0	–	–	–	0	1	0	0	–	–	–	0	1	0	–	–
0	–	–	–	0	1	0	1	–	–	–	0	1	1	–	–
0	–	–	–	0	1	1	0	–	–	–	1	0	0	–	–
0	–	–	–	0	1	1	1	–	–	–	1	0	1	–	–
0	–	–	–	1	0	0	0	–	–	–	0	1	0	–	–
0	–	–	–	1	0	0	1	–	–	–	0	1	1	–	–
0	–	–	–	1	0	1	0	–	–	–	1	0	0	–	–
0	–	–	–	1	0	1	1	–	–	–	1	0	1	–	–
0	–	–	–	1	1	0	0	–	–	–	1	1	0	–	–
0	–	–	–	1	1	0	1	–	–	–	1	1	1	–	–
0	–	–	–	1	1	1	0	–	–	–	1	1	0	–	–
0	–	–	–	1	1	1	1	–	–	–	1	1	1	–	–
1	–	–	–	0	0	0	0	–	–	–	0	0	1	–	–
1	–	–	–	0	0	0	1	–	–	–	0	1	0	–	–
1	–	–	–	0	0	1	0	–	–	–	0	1	1	–	–
1	–	–	–	0	0	1	1	–	–	–	1	0	0	–	–
1	–	–	–	0	1	0	0	–	–	–	1	0	1	–	–
1	–	–	–	0	1	0	1	–	–	–	1	1	0	–	–
1	–	–	–	0	1	1	0	–	–	–	1	1	1	–	–
1	–	–	–	0	1	1	1	–	–	–	1	1	1	–	–
1	–	–	–	1	0	0	0	–	–	–	1	1	1	–	–
1	–	–	–	1	0	0	1	–	–	–	1	1	1	–	–
1	–	–	–	1	0	1	0	–	–	–	1	1	1	–	–
1	–	–	–	1	0	1	1	–	–	–	1	1	1	–	–
1	–	–	–	1	1	0	0	–	–	–	1	1	1	–	–
1	–	–	–	1	1	0	1	–	–	–	1	1	1	–	–
1	–	–	–	1	1	1	0	–	–	–	1	1	1	–	–
1	–	–	–	1	1	1	1	–	–	–	1	1	1	–	–

FIG. 37

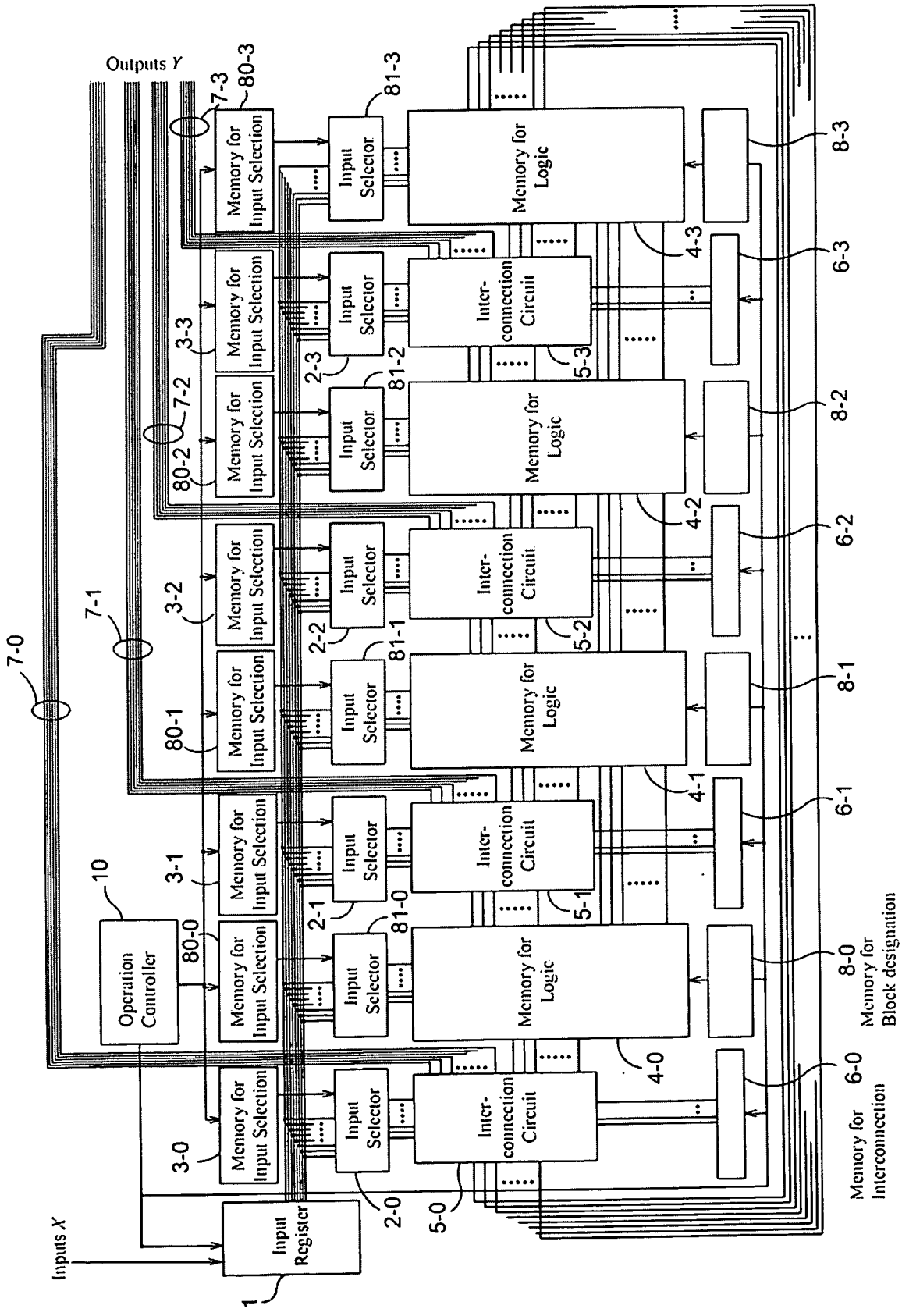

Outputs Y
Inputs X
Operation Controller
Input Register
Memory for Input Selection
Input Selector
Inter-connection Circuit
Memory for Logic
Memory for Block designation
Memory for Interconnection
10
1
7-0
7-1
7-2
7-3
80-0
80-1
80-2
80-3
81-0
81-1
81-2
81-3
2-0
2-1
2-2
2-3
3-0
3-1
3-2
3-3
4-0
4-1
4-2
4-3
5-0
5-1
5-2
5-3
6-0
6-1
6-2
6-3
8-0
8-1
8-2
8-3

FIG. 38

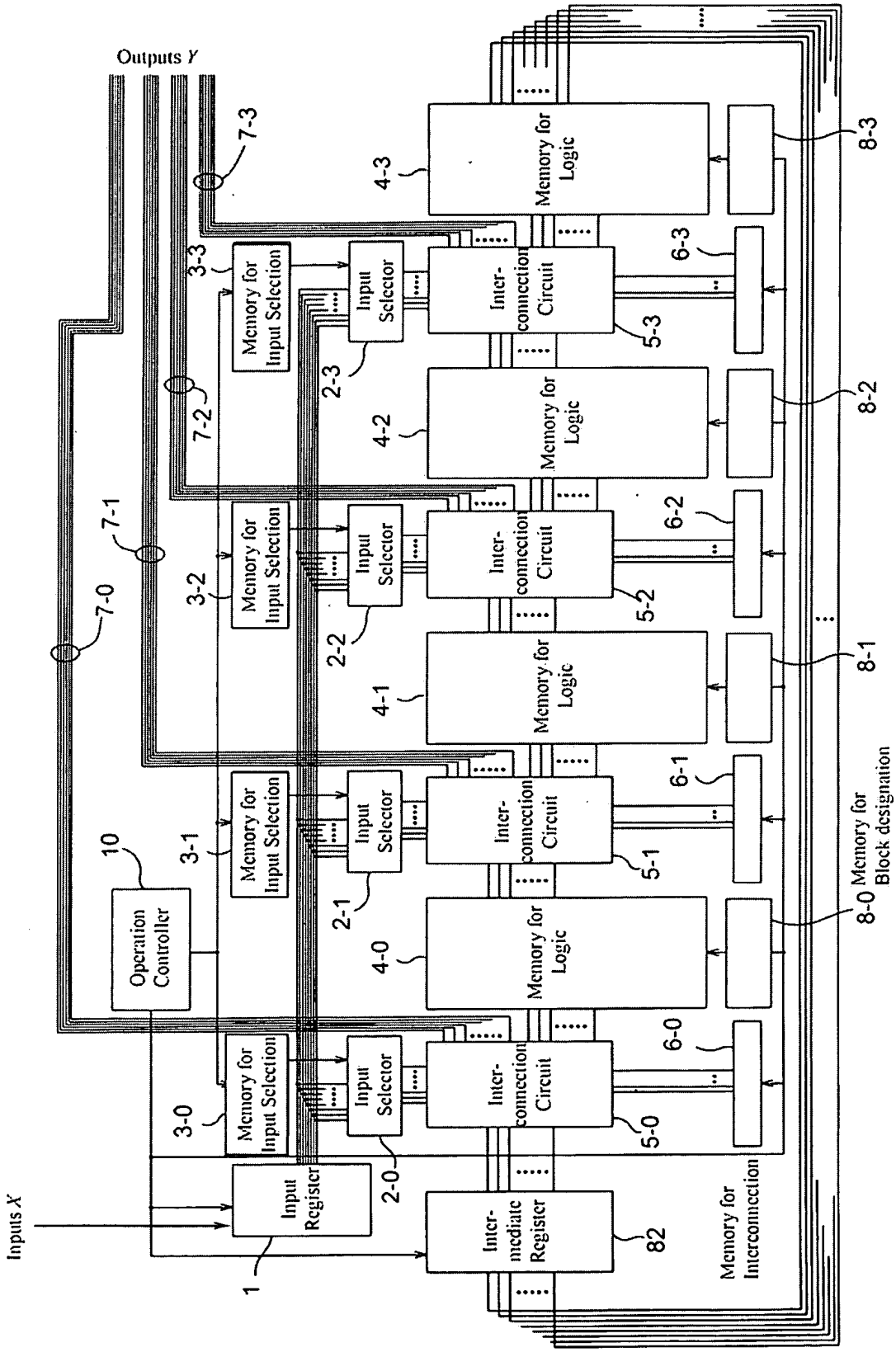

Outputs Y
Inputs X
Input Register
Operation Controller
Memory for Input Selection
Input Selector
Inter-connection Circuit
Memory for Logic
Intermediate Register
Memory for Interconnection
Memory for Block designation

FIG. 39

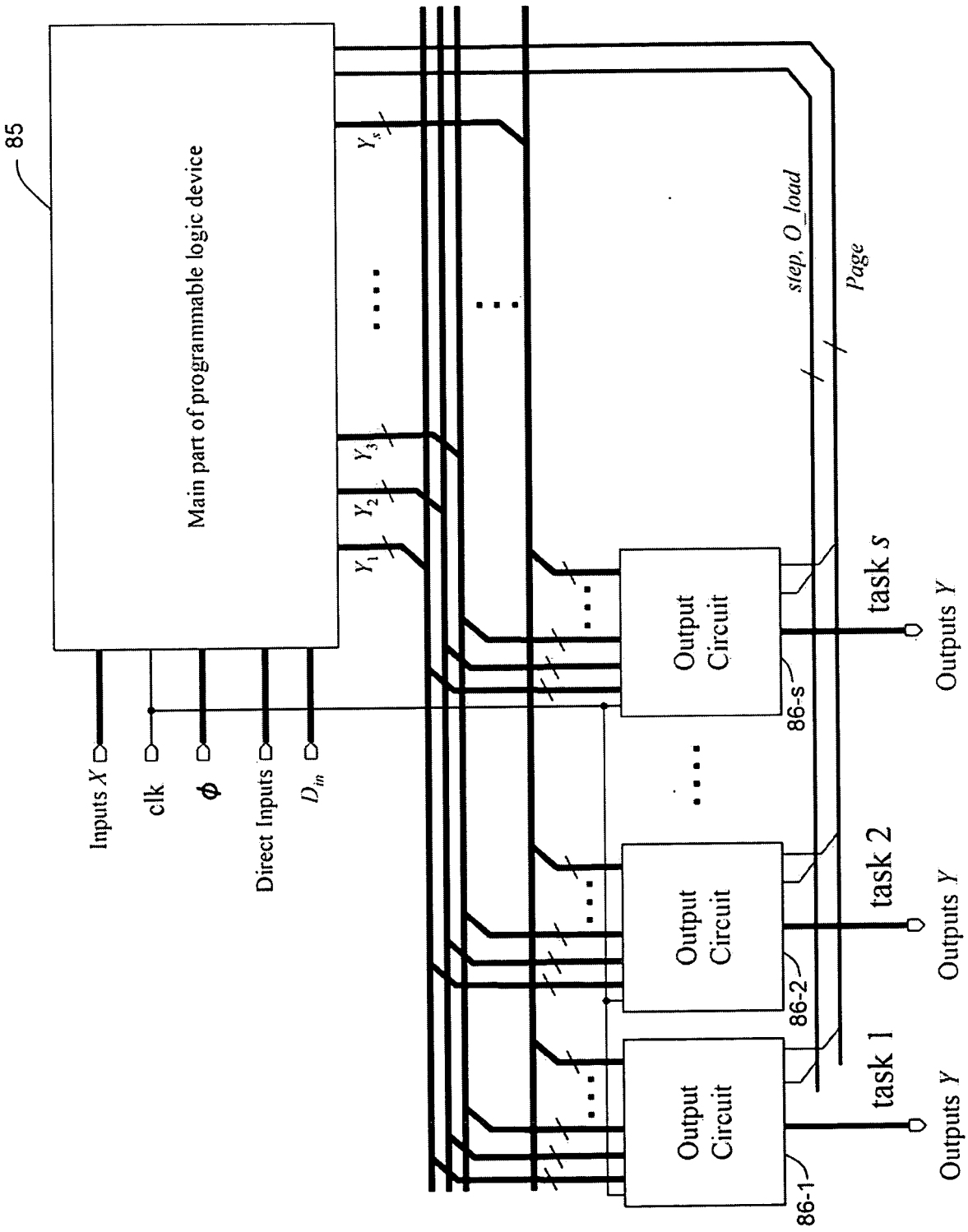

85
Main part of programmable logic device
Y_s
Y_3
Y_2
Y_1
step, O_load
Page
Inputs X
clk
ϕ
Direct Inputs
D_{in}
Output Circuit
86-s
task s
Outputs Y
Output Circuit
86-2
task 2
Outputs Y
Output Circuit
86-1
task 1
Outputs Y

FIG. 40

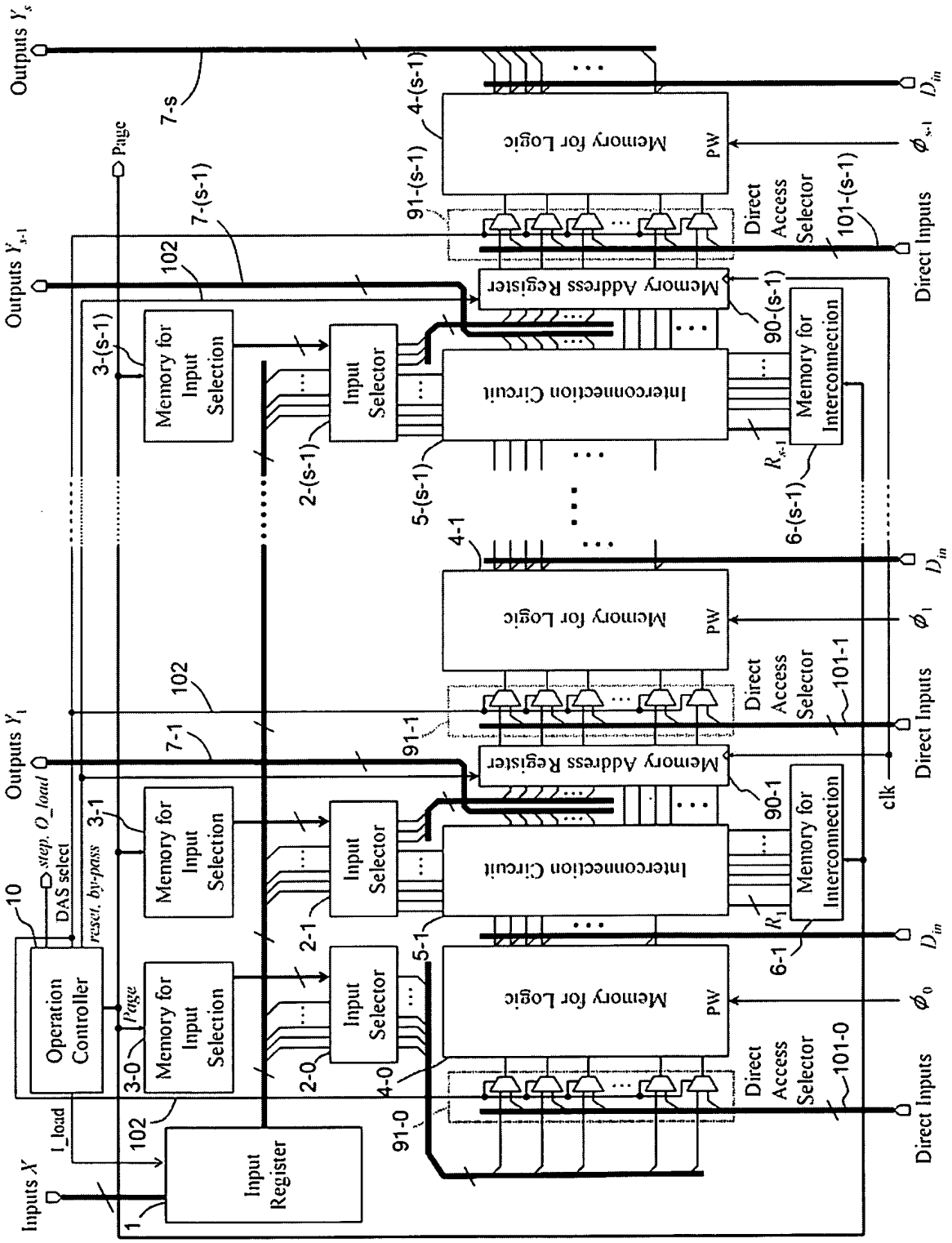

Outputs Y_s
Outputs Y_{s-1}
Outputs Y_1
Outputs Y_0
Page
7-s
7-(s-1)
7-1
7-0
102
Memory for Input Selection
3-(s-1)
3-1
3-0
Input Selector
2-(s-1)
2-1
2-0
Interconnection Circuit
5-(s-1)
5-1
5-0
Memory for Interconnection
90-(s-1)
90-1
90-0
Memory Address Register
91-(s-1)
91-1
91-0
4-(s-1)
4-1
4-0
Memory for Logic
PW
ϕ_{s-1}
ϕ_1
ϕ_0
D_{in}
Direct Access Selector
101-(s-1)
101-1
101-0
Direct Inputs
R_{s-1}
R_1
R_0
6-(s-1)
6-1
6-0
clk
Operation Controller
10
step, O_load
DAS select
reset, by-pass
Page
I_load
Input Register
Inputs X
1

FIG. 41

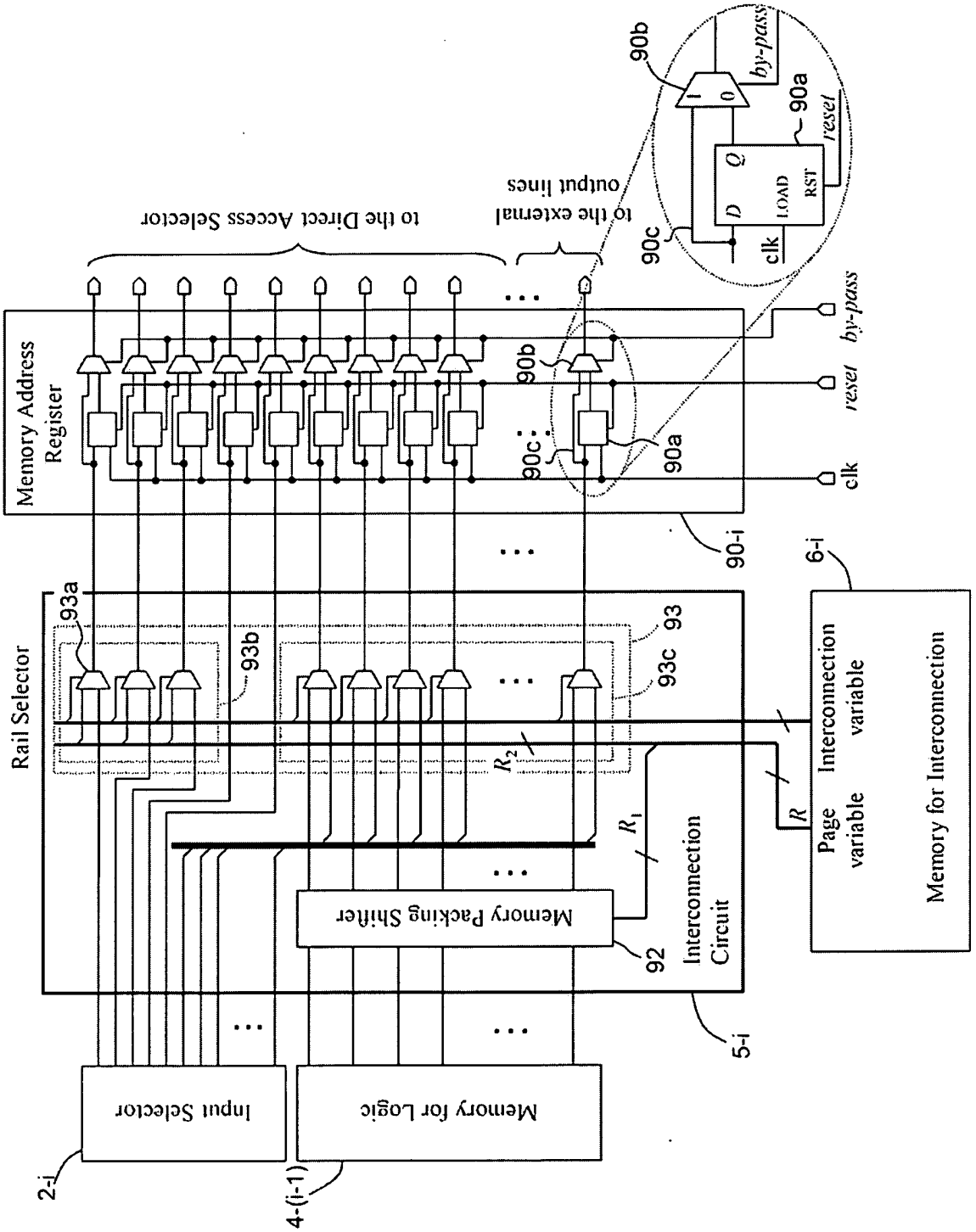

Memory Address Register
Rail Selector
Interconnection Circuit
Memory Packing Shifter
Memory for Logic
Input Selector
Memory for Interconnection
Page variable
Interconnection variable
to the Direct Access Selector
to the external output lines
by-pass
reset
clk
LOAD
RST
90a
90b
90c
90-i
93
93a
93b
93c
92
5-i
6-i
2-i
4-(i-1)

FIG. 42

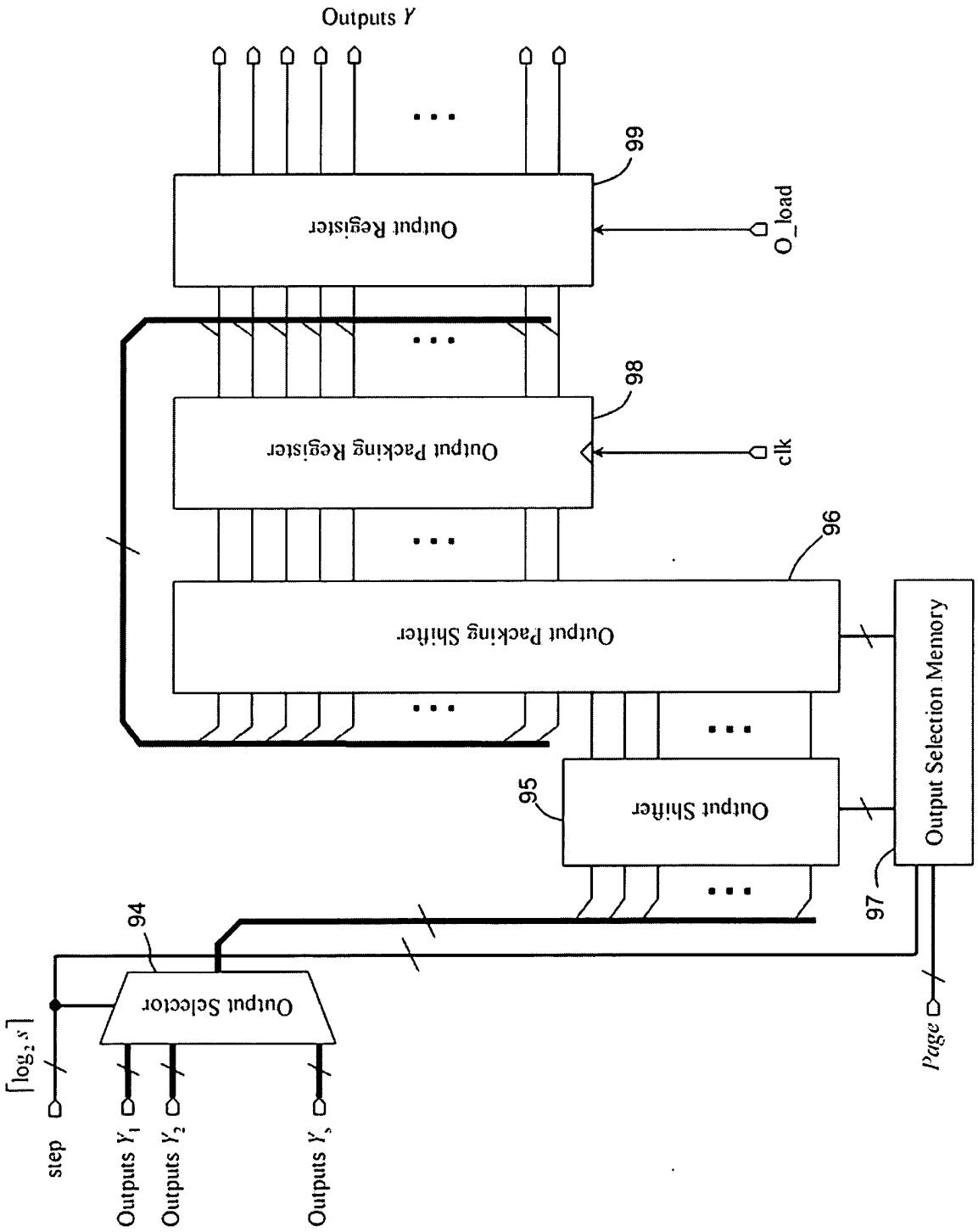

Outputs Y
99
Output Register
O_load
98
Output Packing Register
clk
96
Output Packing Shifter
Output Selection Memory
95
Output Shifter
97
94
Output Selector
Page
step
Outputs Y_1
Outputs Y_2
Outputs Y_s

FIG. 43

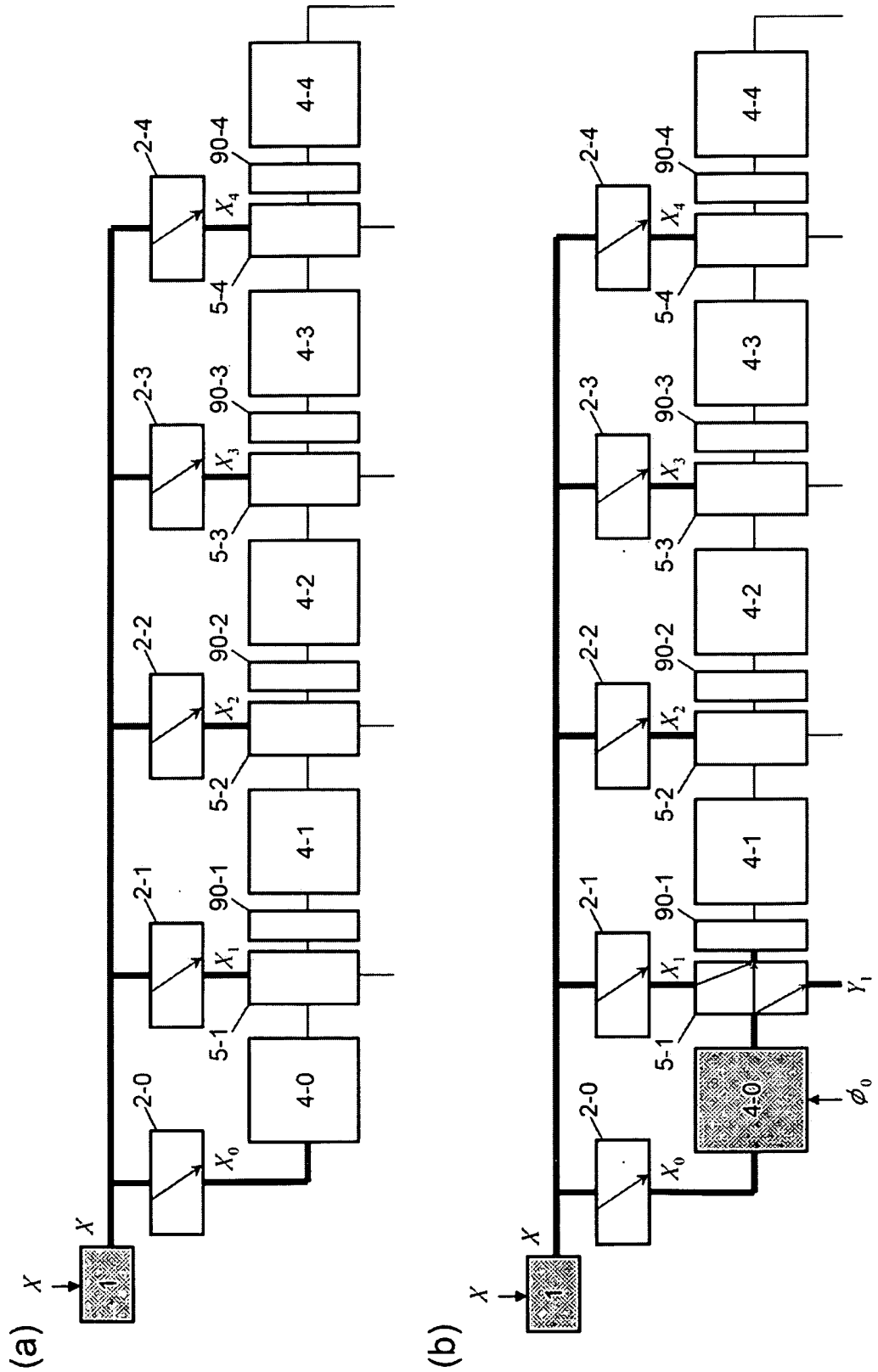

(a)
(b)
X
1
2-0
2-1
2-2
2-3
2-4
X_0
X_1
X_2
X_3
X_4
90-1
90-2
90-3
90-4
5-1
5-2
5-3
5-4
4-0
4-1
4-2
4-3
4-4
Y_1
ϕ_0

FIG. 44

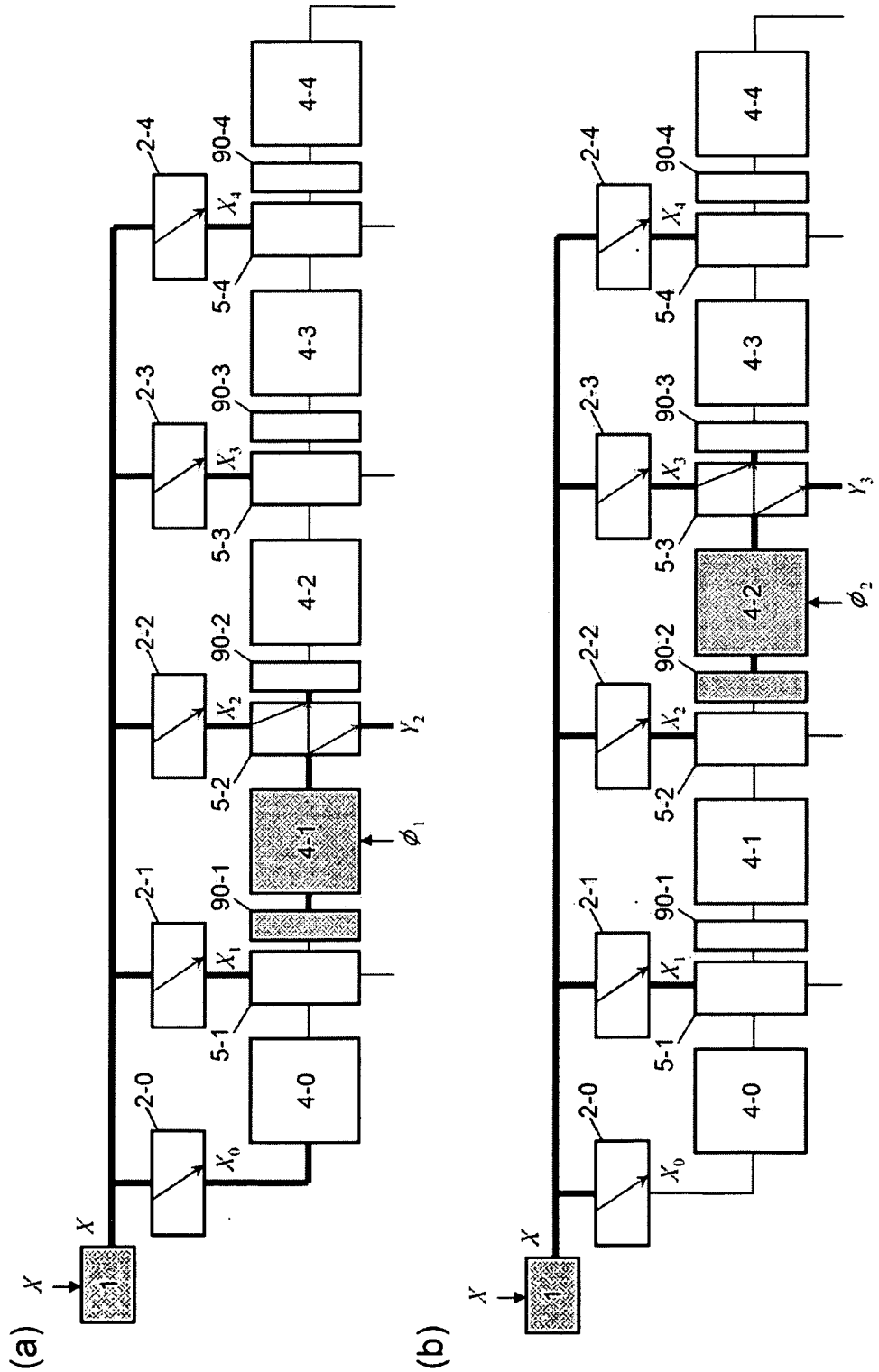

(a)
(b)
X
4-1
2-0
2-1
2-2
2-3
2-4
4-0
4-1
4-2
4-3
4-4
5-1
5-2
5-3
5-4
90-1
90-2
90-3
90-4
X_0
X_1
X_2
X_3
X_4
Y_2
Y_3
ϕ_1
ϕ_2

FIG. 45

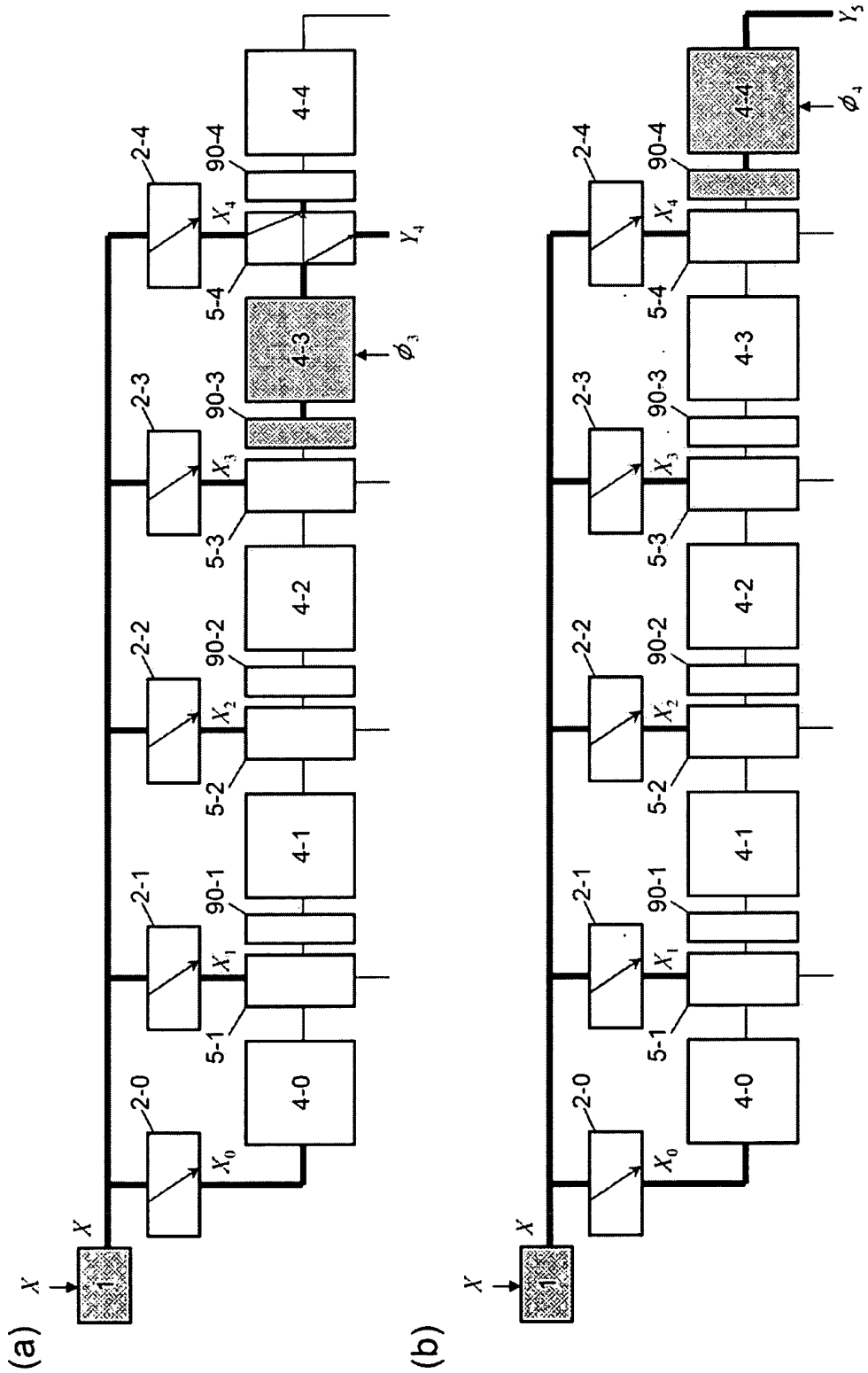

(a)
(b)
X
1
2-0
2-1
2-2
2-3
2-4
X_0
X_1
X_2
X_3
X_4
90-1
90-2
90-3
90-4
4-0
4-1
4-2
4-3
4-4
5-1
5-2
5-3
5-4
ϕ_3
ϕ_4
Y_4
Y_5

FIG. 46

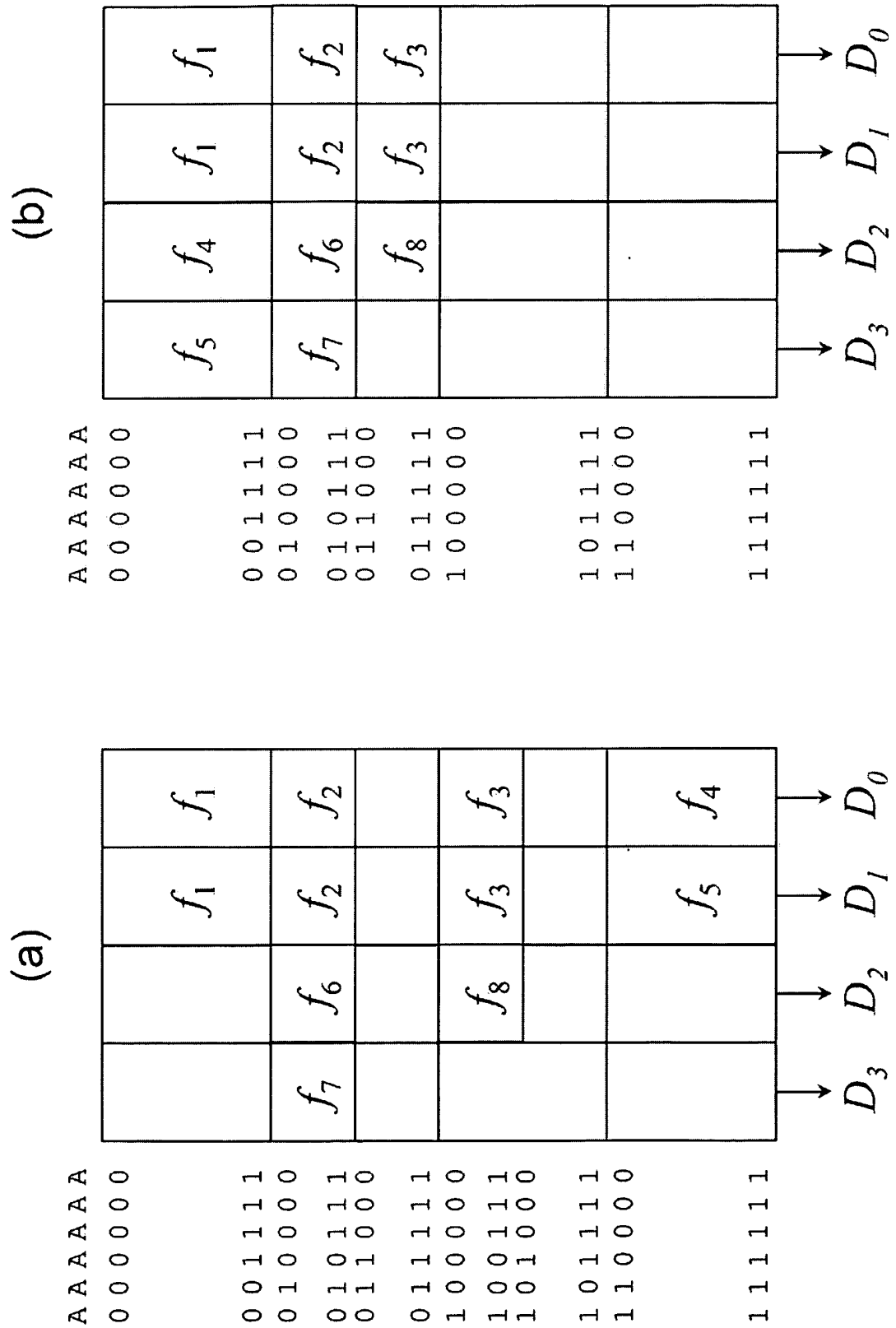

(a)
(b)
AAAAAA
000000
001111
010000
010111
011000
011111
100000
100111
101000
101111
110000
111111
f_1
f_2
f_3
f_4
f_5
f_6
f_7
f_8
D_0
D_1
D_2
D_3

FIG. 47

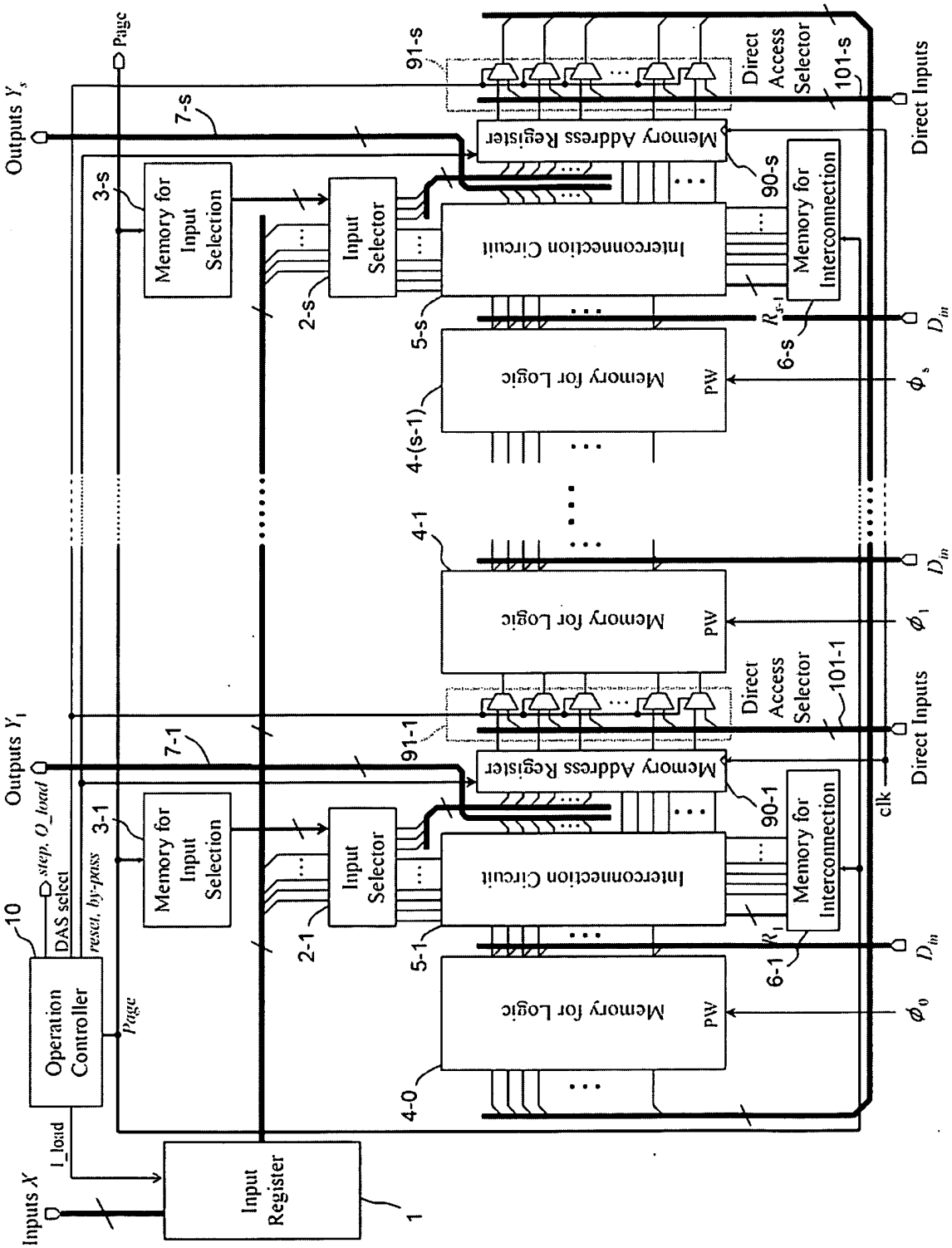

Outputs Y_s
Page
7-s
91-s
Direct Access Selector
101-s
Direct Inputs
Memory Address Register
90-s
3-s
Memory for Input Selection
Input Selector
2-s
Interconnection Circuit
Memory for Interconnection
5-s
R_{s-1}
6-s
D_{in}
Memory for Logic
PW
ϕ_s
4-(s-1)
4-1
ϕ_1
Outputs Y_1
7-1
91-1
101-1
90-1
3-1
2-1
5-1
R_1
6-1
ϕ_0
4-0
clk
step, O_load
DAS select
reset, by-pass
10
Operation Controller
Page
I_load
Inputs X
Input Register
1

FIG. 48

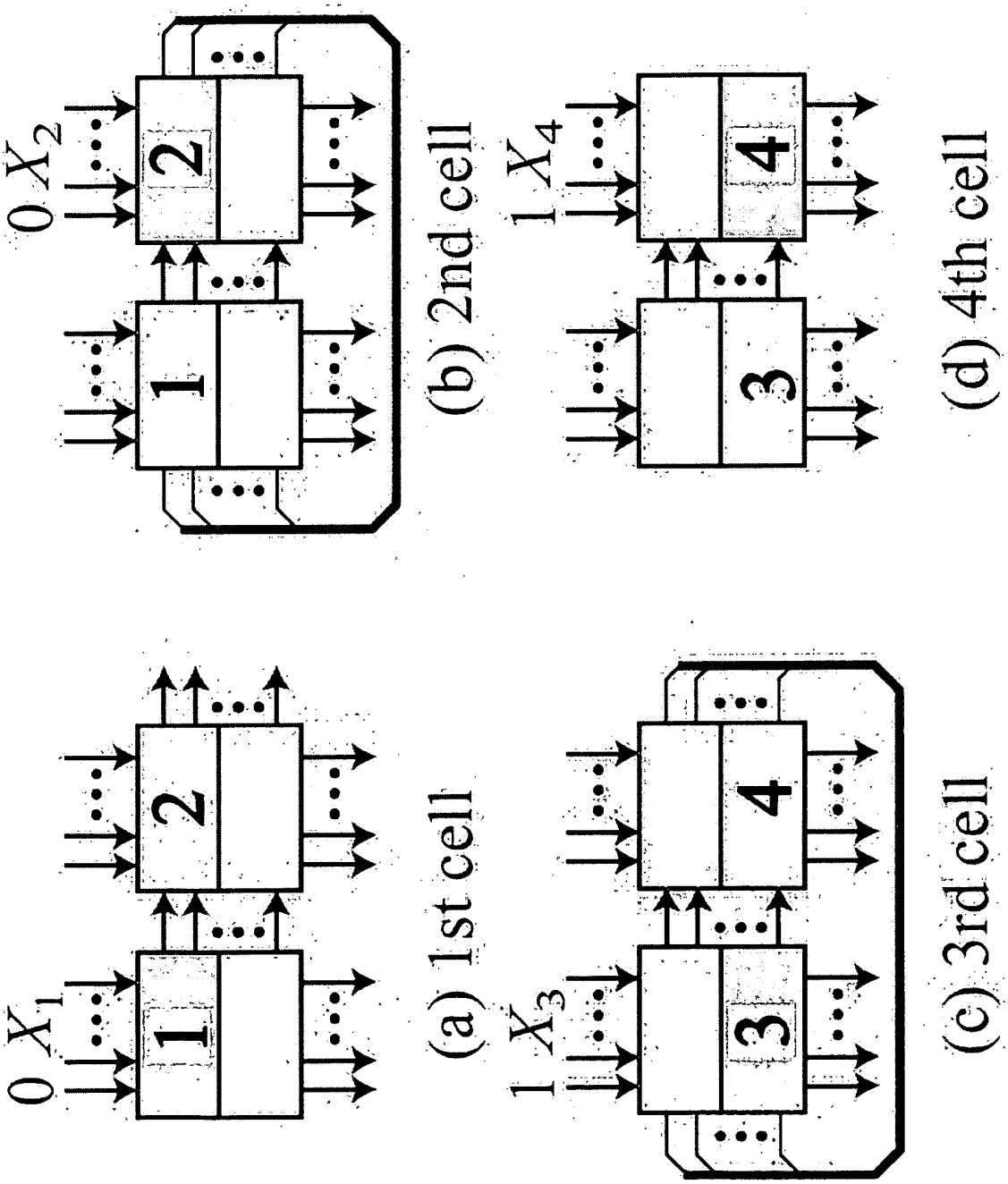

0 X_1
1
2
(a) 1st cell
0 X_2
1
2
(b) 2nd cell
1 X_3
3
4
(c) 3rd cell
1 X_4
3
4
(d) 4th cell

FIG. 49

(a)
$f = ((x_1 \vee x_2)x_3 \vee x_4)x_5 \vee x_6$
1
x1
AND
x2
OR
x3
AND
x4
OR
x5
AND
x6
OR
f
(x1,x2,x3,x4,x5,x6) is the optimal ordering for this function.
(b)
$g = ((x_4x_5 \vee x_6)x_1 \vee x_2)x_3$
0
x4
OR
x5
AND
x6
OR
x1
AND
x2
OR
x3
AND
g
(x4,x5,x6,x1,x2,x3) is the optimal ordering for this function.

FIG. 50

$$f = (((x_1 \vee x_2)x_3 \vee x_4)x_5 \vee x_6$$

$$g = (((x_4 x_5 \vee x_6)x_1 \vee x_2)x_3$$

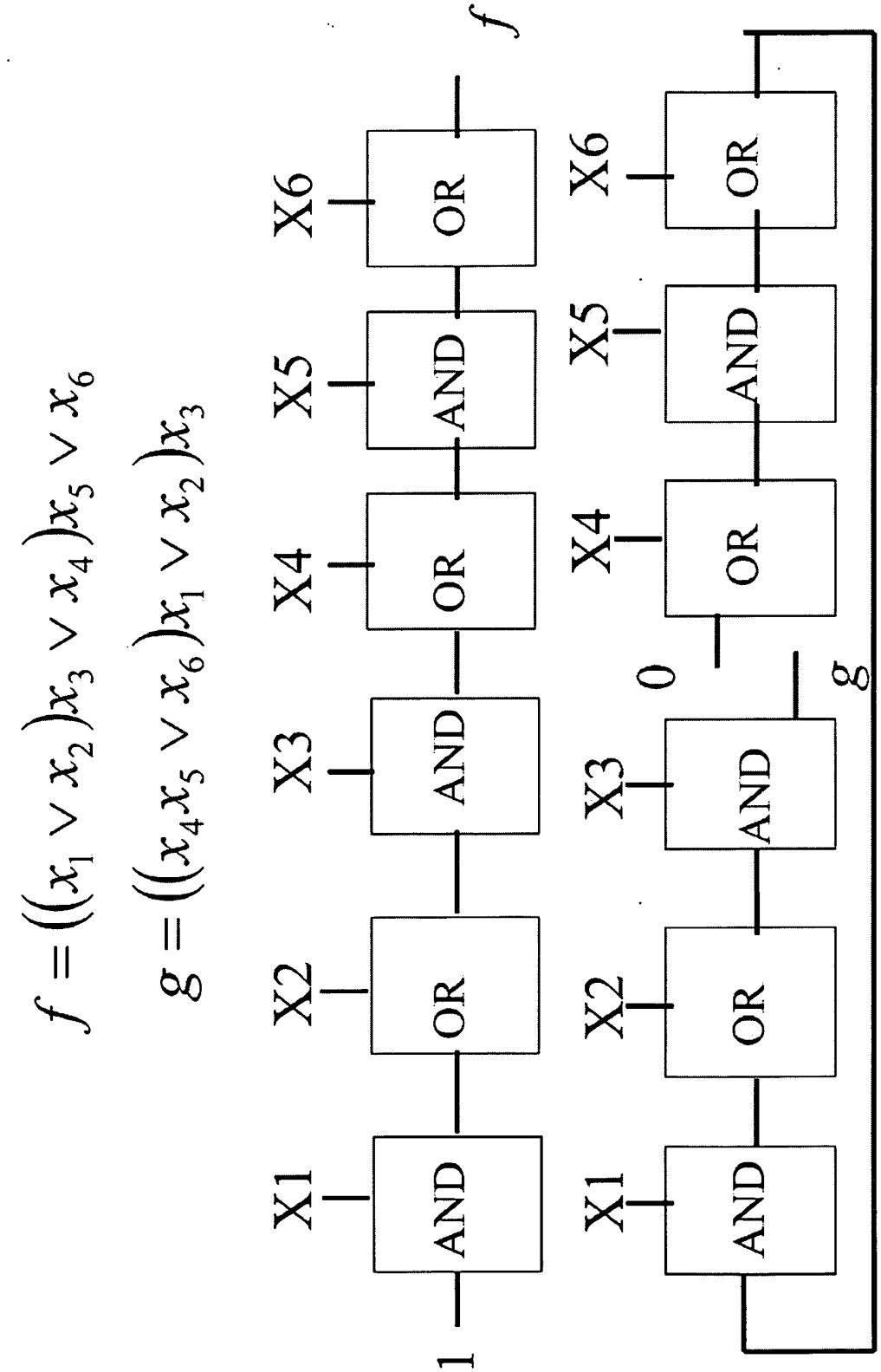
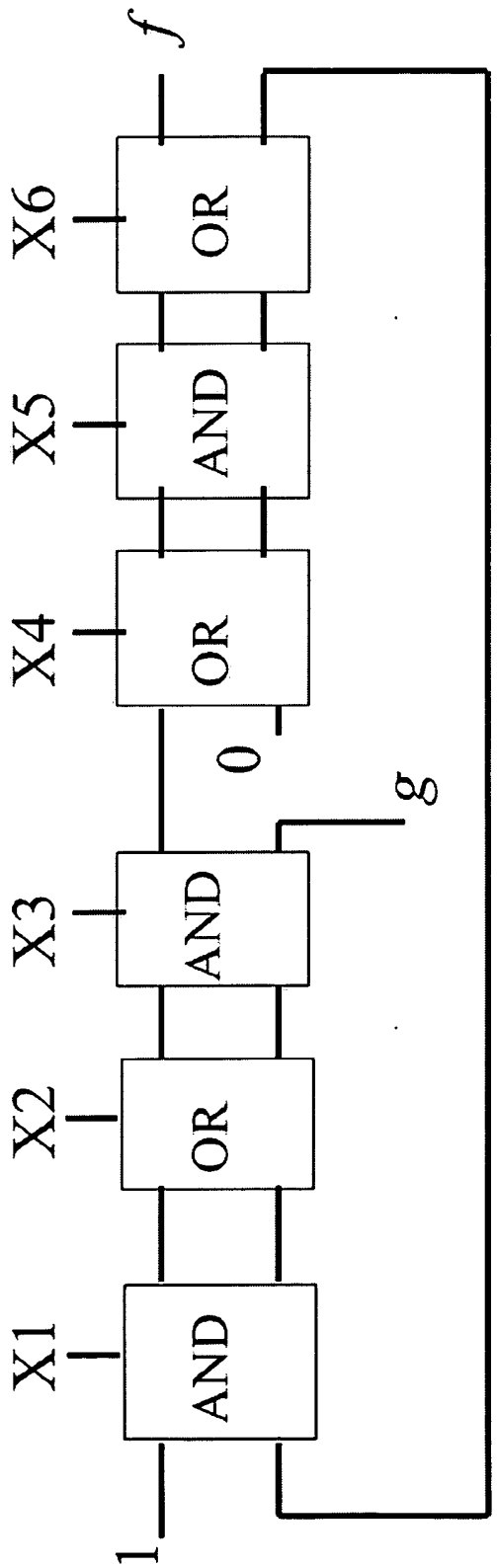


FIG. 51

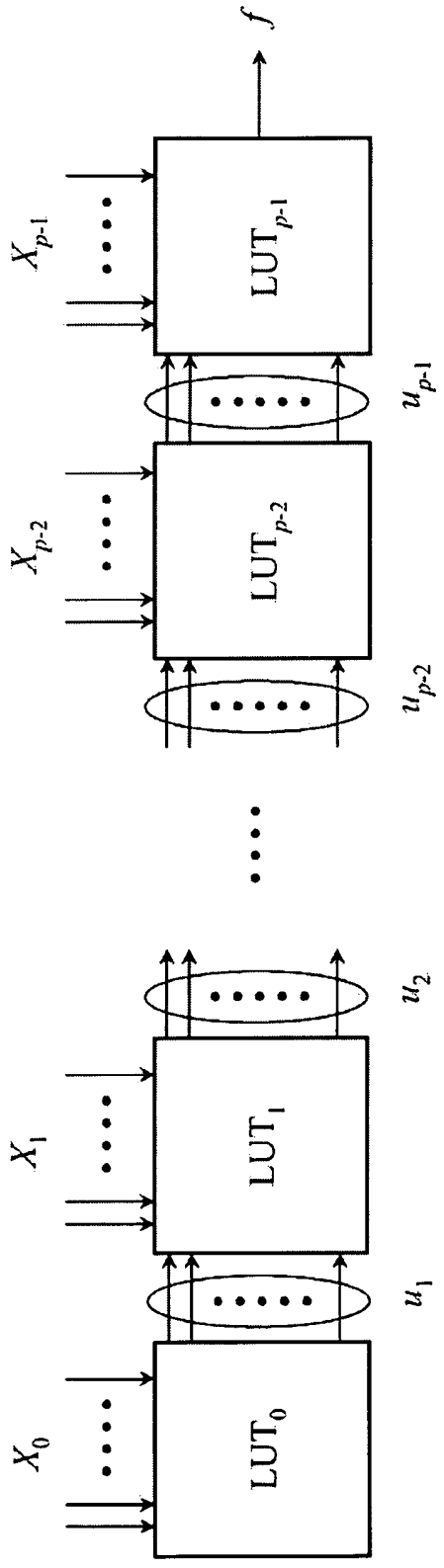
$$f = (((x_1 \vee x_2)x_3 \vee x_4)x_5 \vee x_6$$

$$g = (((x_4 x_5 \vee x_6)x_1 \vee x_2)x_3$$



By using the LUT ring, the ordering can be optimal for two functions.

FIG. 52



LUT cascade with p memory cells